Lapis 0.20um SOI Process
1.8V I/O Library Release Note

v.3.0 2025.3.18

Approved by	I. Kurachi (KEK)
Verified by	Y. Arai (KEK)
ESD Counseled by	Y. Fukuda (RCJ)
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Revision History

Rev	Date	Notice	Description
0.0	2020.03.31		新規作成
1.0	2020.11.16		Typo修正：4-4、4-5 Truth Table
2.0	2023.7.24	Y. Arai	Added BN5 under BNW to support more rigid back-side potential. Removed double SOI related error.
3.0	2024.11.15	Y. Arai	Added enhanced driving capability & better linearity version of analog buffer (io_aobuf4_1P8 & io_aobufar_1P8).

Contents

1. Introduction

- This library is converted from ‘IOLIBP1’ 3.3V I/O prepared for p-type substrate and using single 1.8V power supply.
- Please note cells in the library are just shown as samples and its performance is not guaranteed, so please use these cells at your own risk.
- GDS layout and schematics are contained in the 'IOLIBP1_1P8_v3.tar.gz', so please define this library as 'IOLIBP1_1P8' in cds.lib file as
  'DEFINE IOLIBP1_1P8 ./IOLIBP1_1P8_v3’.
- If you find any error in the library, please notify to takayana@post.kek.jp or yasuo.arai@kek.jp

2. Specification

2-1. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power-supply Voltage	VDD18	-0.3～ +2.5	V
Input Voltage	Vin	-0.3 ～ VDD18+0.3	V
Output Voltage	Vout	-0.3 ～ VDD18+0.3	V
Storage Temperature	Tstg	-55 ～ +125	℃

2-2. Recommended Operating Conditions

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Power-supply Voltage	VDD18	1.65	1.8	1.95	V
Operating Temperature	Top	-40		125	℃

2. Specification

2-3. DC Characteristic for digital buffers

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Input Voltage(High-Level)	VIH	0.7 X VDD18	-	VDD18	V
Input Voltage(Low-Level)	VIL	0	-	0.3 X VDD18	V
Output Voltage(High-Level)	VOH	0.75 X VDD18	-	VDD18	V
Output Voltage(Low-Level)	VOL	0	-	0.25 X VDD18	V
Input Current(High-Level)	IIH	-	-	1.0	μA
Input Current(Low-Level)	IIL	-1.0	-	-	μA
Output Current(Z/High-Level)	IOZH	-	-	1.0	μA
Output Current(Z/Low-Level)	IOZL	-1.0	-	-	μA

2. Specification

2-4. AC Characteristic

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Input buffer Propagated Delay Time	TpHL	-	-	1.5	ns
	TpLH	-	-	1.5	ns
Output buffer Propagated Delay Time	TpHL	-	-	5.0	ns
	TpLH	-	-	5.0	ns

2-5. ESD Target

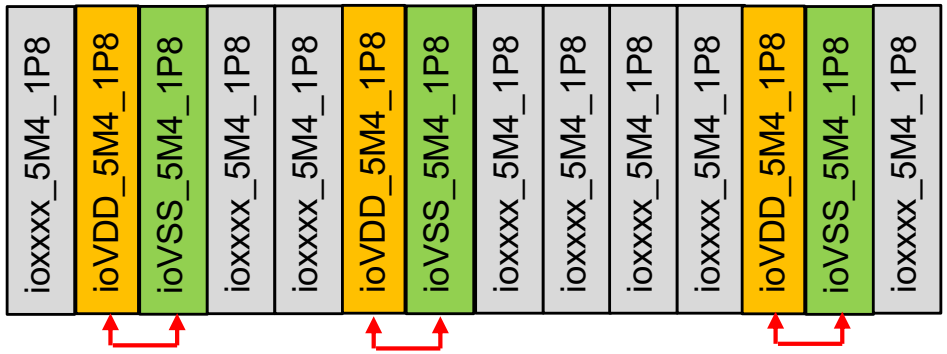
Parameter	Symbol	Value	Unit
HBM(Human Body Model)	HBM	±2000	V
CDM(Charge Device Model)	CDM	±500	V

2. Specification

2-6.ESD Rules

(a) Power/GND Cell

Please put Power Cell(“ioVDD18_5M4_1P8”) next to GND Cell(“ioVSS_5M4_1P8).



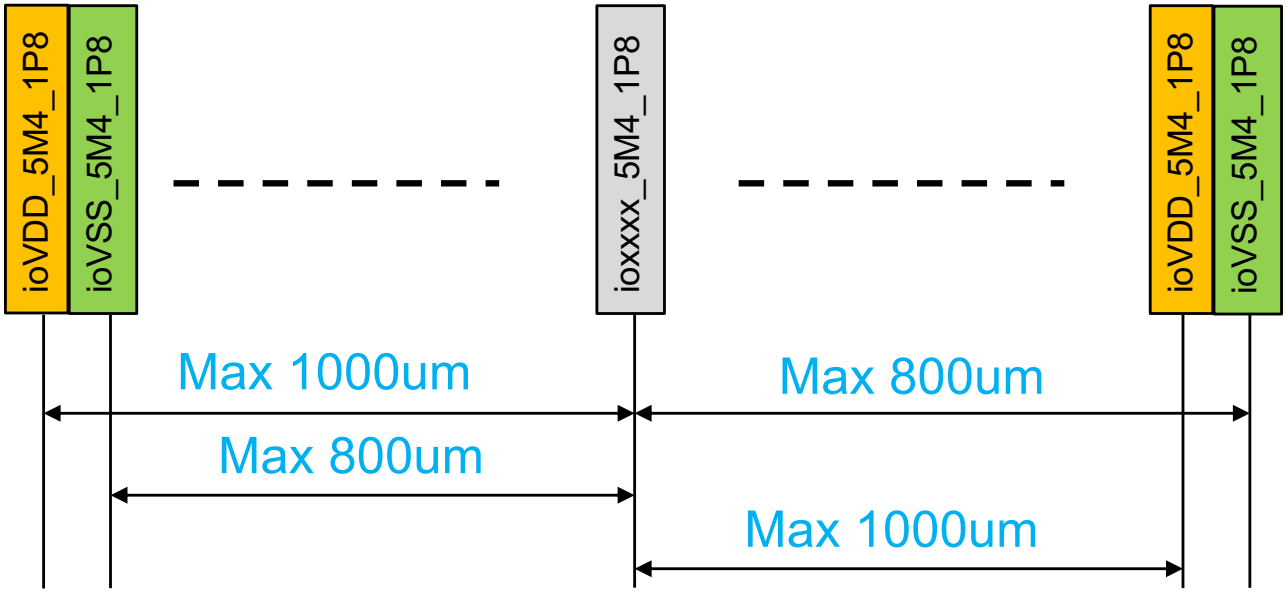
2. Specification

2-6.ESD Rules

(b) Input/Output Cell

Please put I/O Cell as follows.

The maximum distance from I/O to “ioVDD_5M4_1P8” is 1000μm.
The maximum distance from I/O to “ioVSS_5M4_1P8” is 800μm



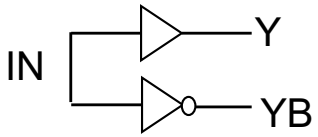
3. Cell list

Status	1P8 IO Library			Status		
1.8V対応	Cell name	Type	Description	schematic	layout	lvs/drc
○	ioIT4N_5M4_1P8	Input	1.8V LVTTL Digital Input Buffer with Y,YB	○	○	○
○	ioIT4ND_5M5_1P8	Input	1.8V LVTTL Digital Input Buffer with Y,YB and Pull Down Tr (~17uA@1.8V)	○	○	○
○	ioIT4NDP_5M5_1P8	Input	1.8V LVTTL Digital Input Buffer with Y,YB and Pull Down Tr (~17uA@1.8V) Enhanced Y,YB	○	○	○
○	ioOT4A_5M5_1P8	Output	Tri-state Digital Output Buffer (4mA)	○	○	○
○	ioOT4B_5M5_1P8	Output	Tri-state Inverting Digital Output Buffer (4mA)	○	○	○
○	ioVDD18_5M4_1P8	Power	1.8V Power cell for core transistors	○	○	○
○	ioVSS_5M4_1P8	GND	Ground cell for VDD18	○	○	○
○	ioCORNER_5M6_1P8	-	Corner Cell	○	○	○
○	iodr_5M4_1P8	Input/Outout	Analog pad with protection diodes and resistor	○	○	○
○	iod_5M4_1P8	Input/Outout	Analog pad with protection diodes	○	○	○
○	iothr_5M4_1P8	Input/Outout	Direct analog pad	○	○	○
○	iobuf_5M4_1P8	Input/Outout	Digital bidirectional Input/Output (4mA) Buffer	○	○	○
○	iobuf2_5M4_1P8	Input/Outout	Digital bidirectional Input/Output (4mA) Buffer with fast return path from A to Y.	○	○	○
○	iofill_5M4_1P8	-	IO ring fill cell.	○	○	○
○	iofill_M4cut_1P8	-	IO ring fill cell. Layer change in M4 power line.	○	○	○
○	ioAOBUF18EN3_5M4_RR_VF	Output	Analog output buffer	○	○	○
○	ioBIAS18_5M4_RR	-	Analog buffer bias circuit	○	○	○
○	io_aobuf_1P8	-	Analog buffer layout example	○	○	○
○	ioring29_5M5_1P8	-	IO ring for 2.9mm chip (PGA178)	○	○	○
○	ioring29L2_5M5_1P8	-	IO ring for 2.9mm chip with 200um bias spacing for pixel (PGA178)	○	○	○
○	ioring45_5M5_1P8	-	IO ring for 4.5mm chip (PGA178)	○	○	○
○	ioring45L2_5M5_1P8	-	IO ring for 4.5mm chip with 200um bias spacing for pixel (PGA178)	○	○	○
○	ioring60_5M5_1P8	-	IO ring for 6.0 mm chip (PGA240)	○	○	○
○	ioring60L2_5M5_1P8	-	IO ring for 6.0 mm chip with 200um bias spacing for pixel (PGA240)	○	○	○
○	ioring60L2S_5M5_1P8	-	IO ring for 6.0 mm chip with 200um bias spacing for pixel (PGA178)	○	○	○
○	**Io_aobuf4_1P8 (new)**	**Output**	**Analog buffer layout example (Enhanced Driving capability)**	**○**	**○**	**○**
○	**Io_aobufar_1P8 (new)**	**Output**	**Analog buffer layout example (Enhanced Driving capability、Better Linearity)**	**○**	**○**	**○**

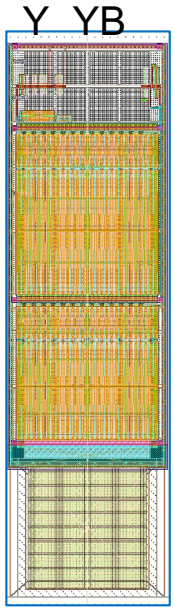
4. I/O Buffer cells

4-1. ioIT4N_5M4_1P8 (digital input buffer)

Logic Symbol



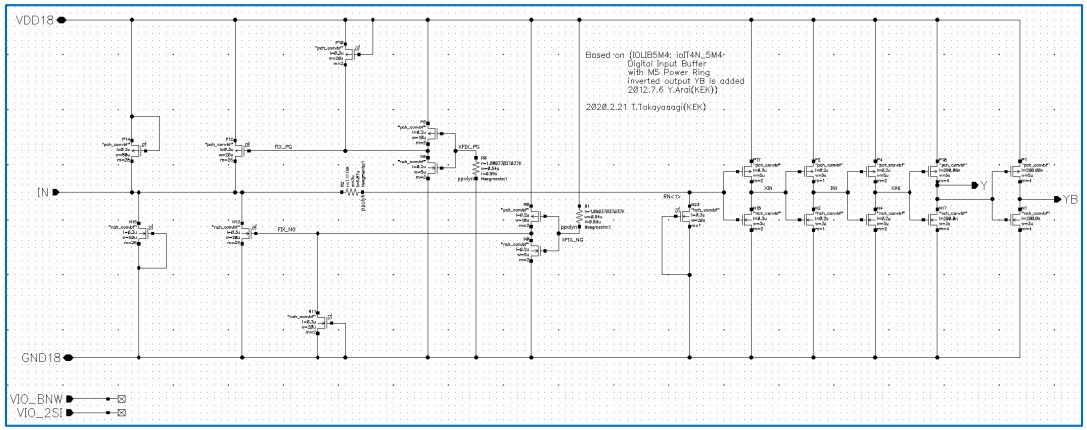
Layout



Truth Table

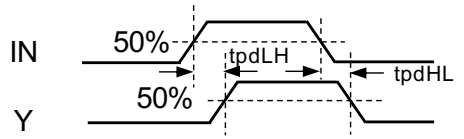
Input IN	Output Y	Output YB
1	1	0
0	0	1

Schematic



Delay (c+cc post Simulation Result)

From	To	Tpd	Tpd(ns)
IN	Y	LH	0.36
		HL	0.44
IN	YB	LH	0.60
		HL	0.68

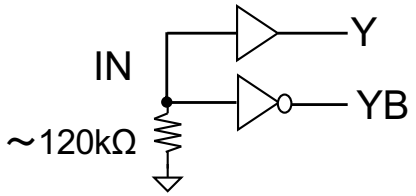


<Condition> Tr:Typical, VDD18=1.8V, Tj=25deg, F=100MHz, Cload= 0.4pF

4. I/O Buffer cells

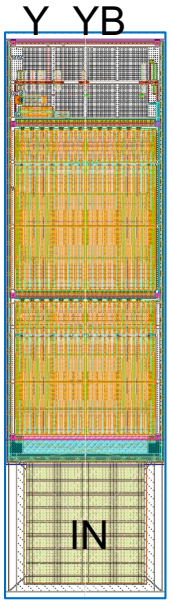
4-2. ioIT4ND_5M5_1P8 (digital input buffer with pull down)

Logic Symbol



I(Pull Down)=15μA@VIN=1.8V

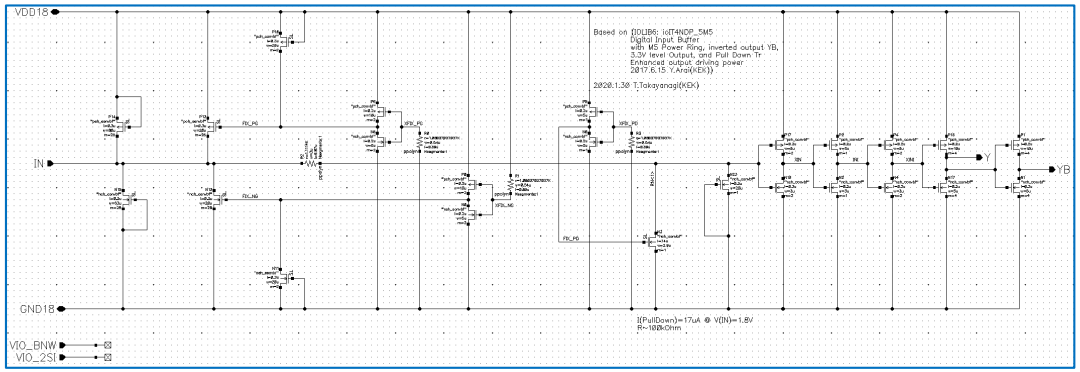
Layout



Truth Table

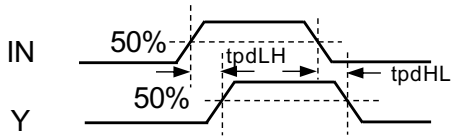
Input IN	Output Y	Output YB
1	1	0
0	0	1

Schematic



Delay (c+cc post Simulation Result)

From	To	Tpd	Tpd(ns)
IN	Y	LH	0.39
		HL	0.45
IN	YB	LH	0.64
		HL	0.68

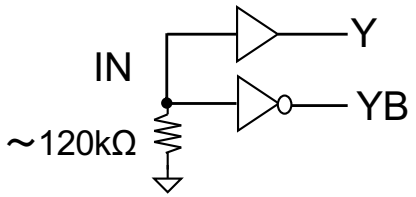


<Condition> Tr:Typical, VDD18=1.8V, Tj=25deg, F=100MHz, Cload= 0.4pF

4. I/O Buffer cells

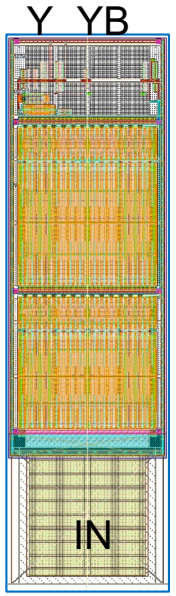
4-3. ioIT4NDP_5M5_1P8 (digital input buffer with pull down Enhanced Y,YB)

Logic Symbol



I(Pull Down)=15μA@VIN=1.8V

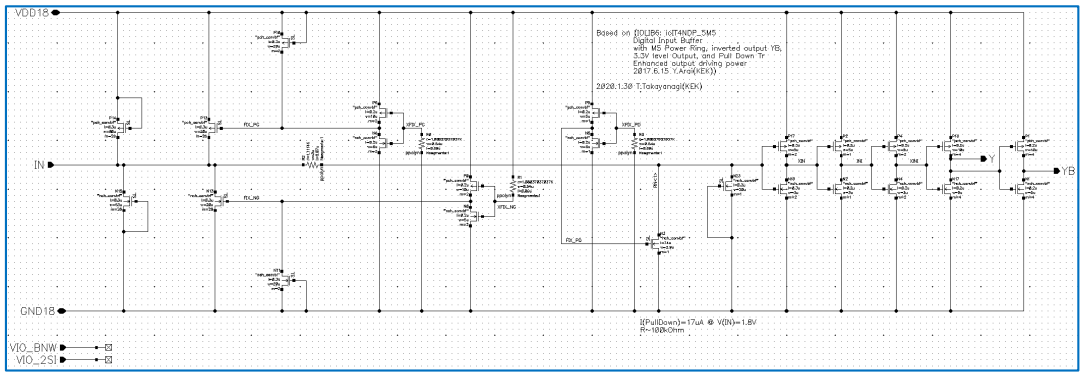
Layout



Truth Table

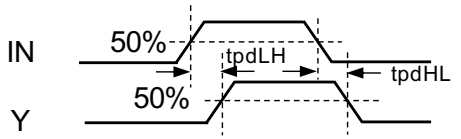
Input IN	Output Y	Output YB
1	1	0
0	0	1

Schematic



Delay (c+cc post Simulation Result)

From	To	Tpd	Tpd(ns)
IN	Y	LH	0.38
		HL	0.42
IN	YB	LH	0.53
		HL	0.56

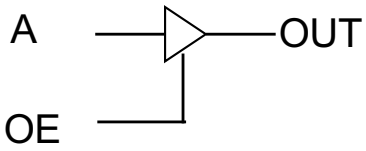


<Condition> Tr:Typical, VDD18=1.8V, Tj=25deg, F=100MHz, Cload= 0.4pF

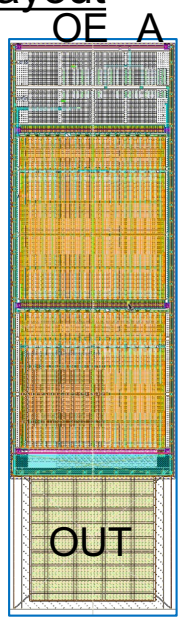
4. I/O Buffer cells

4-4. ioOT4A_5M5_1P8 (Tri-state Digital Output Buffer (4mA))

Logic Symbol



Layout



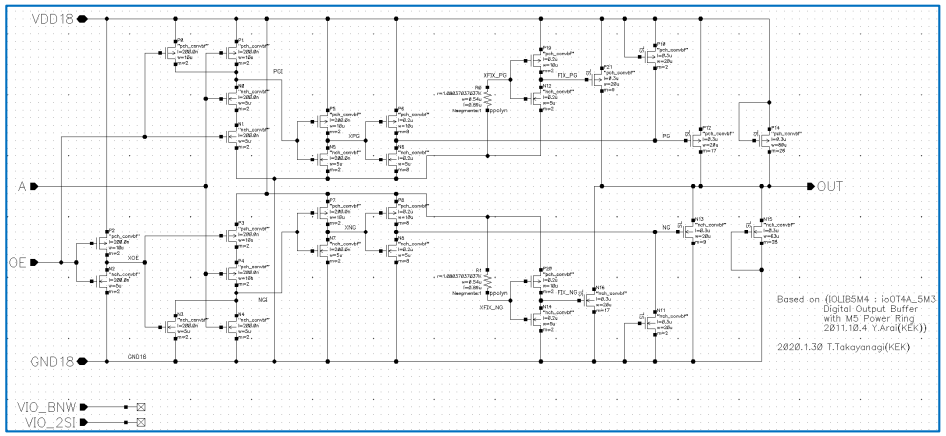
Truth Table

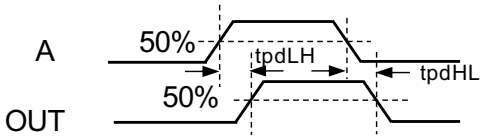
Input A	Input OE	Output OUT
1	1	1
0	1	0
X	0	Z

Delay (c+cc post Simulation Result)

From	To	Tpd	Tpd(ns)
A	OUT	LH	0.79
		HL	1.33

Schematic



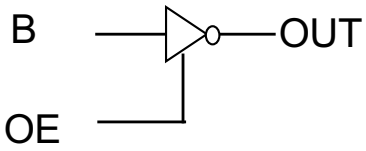


<Condition> Tr:Typical, VDD18=1.8V,
Tj=25deg, F=60MHz, Cload= 25pF

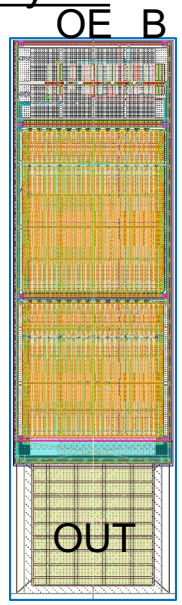
4. I/O Buffer cells

4-5. ioOT4B_5M5_1P8 (Tri-state Inverting Digital Output Buffer (4mA))

Logic Symbol



Layout



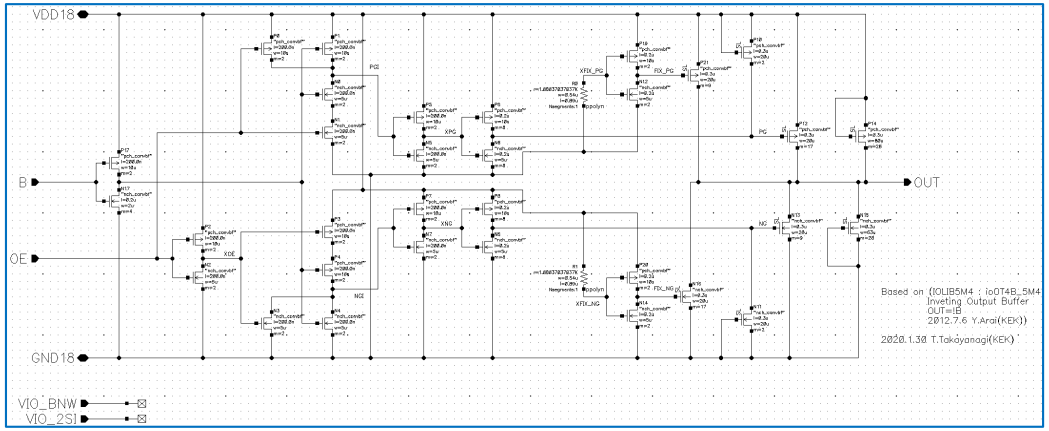
Truth Table

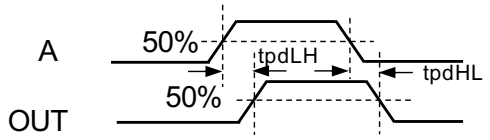
Input B	Input OE	Output OUT
1	1	0
0	1	1
X	0	Z

Delay (c+cc post Simulation Result)

From	To	Tpd	Tpd(ns)
B	OUT	LH	0.84
		HL	1.43

Schematic



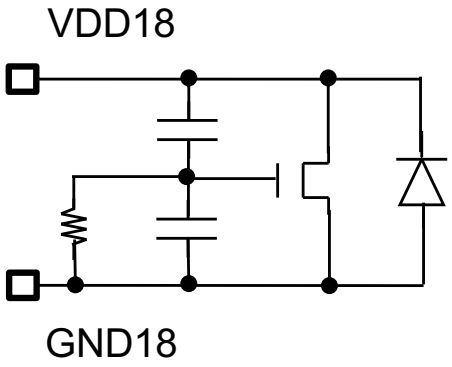


<Condition> Tr:Typical, VDD18=1.8V,
Tj=25deg, F=60MHz, Cload= 25pF

4. I/O Buffer cells

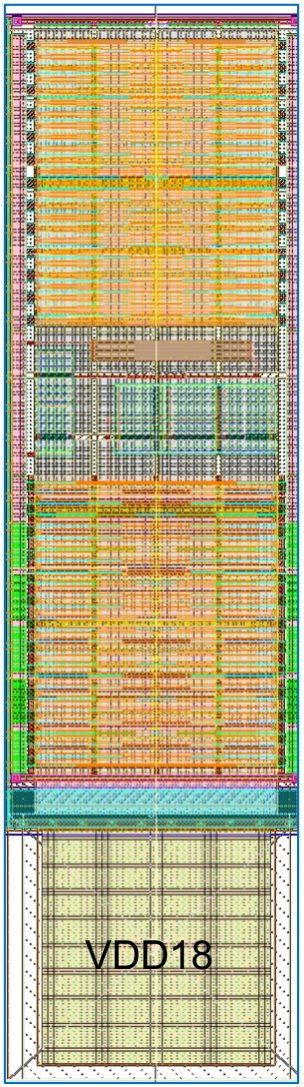
4-6. ioVDD18_5M4_1P8 (1.8V Power cell for core transistors)

Logic Symbol

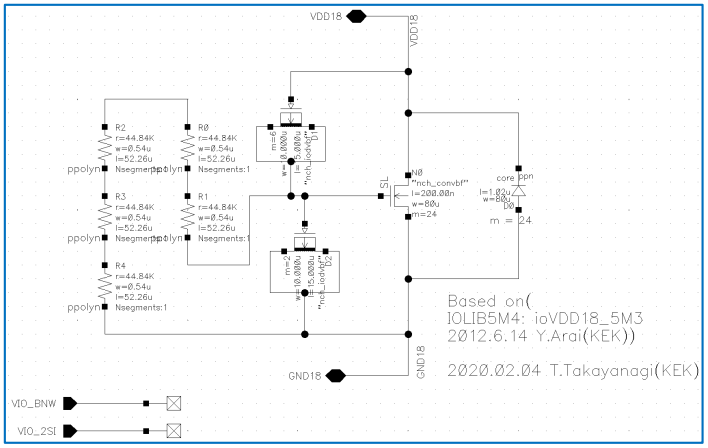


CC Timer Power Clamp

Layout



Schematic



4. I/O Buffer cells

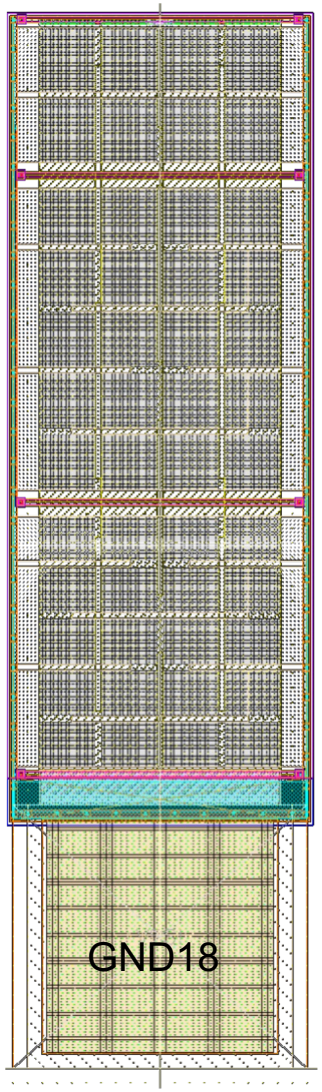
4-7. ioVSS_5M4_1P8 (Ground cell for VDD18)

Logic Symbol

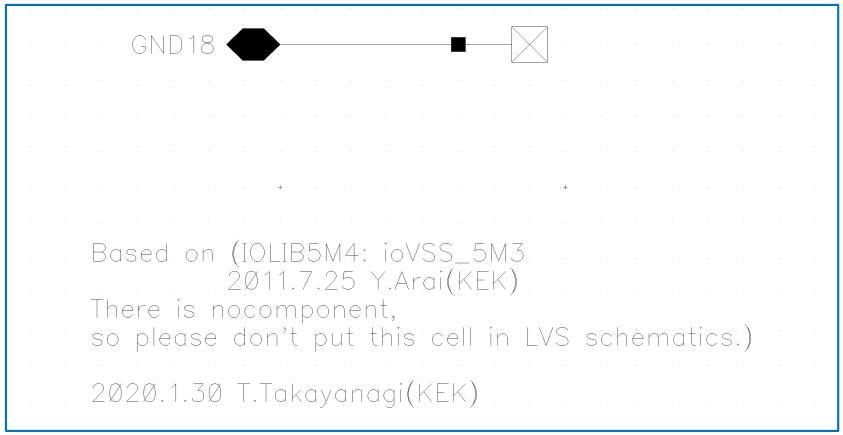
- GND18

There is no internal circuit so not need to include in schematic for LVS check.

Layout



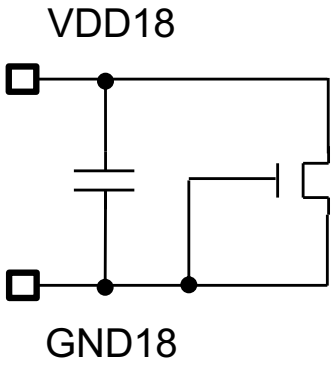
Schematic



4. I/O Buffer cells

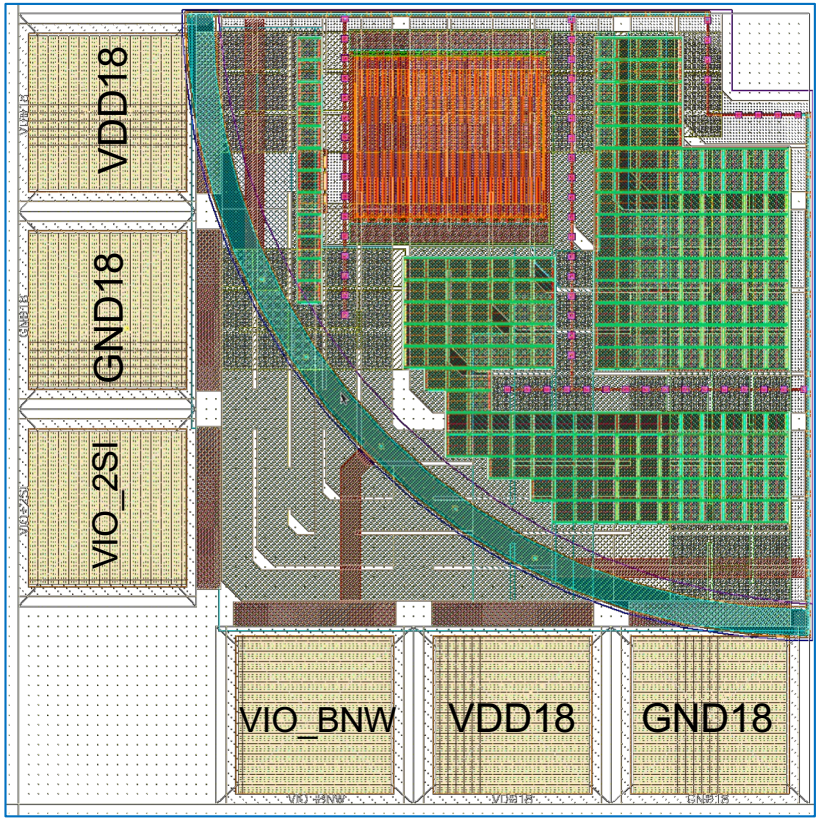
4-8. ioCORNER_5M6_1P8 (Corner Cell)

Logic Symbol

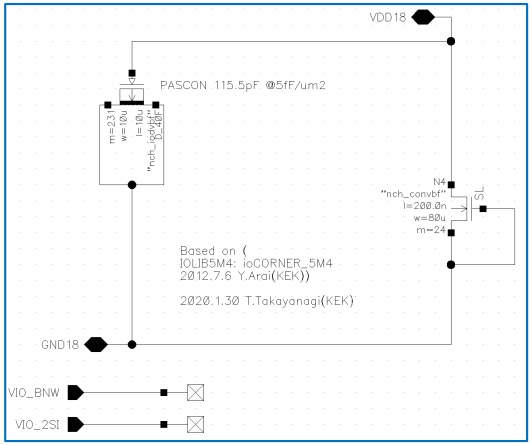


In addition to power and ground pads, this cell contains BPW(VIO_BNW) and SOI2(VIO_2SI) pads which are connected to BNW and SOI2 layer in I/O buffers.

Layout



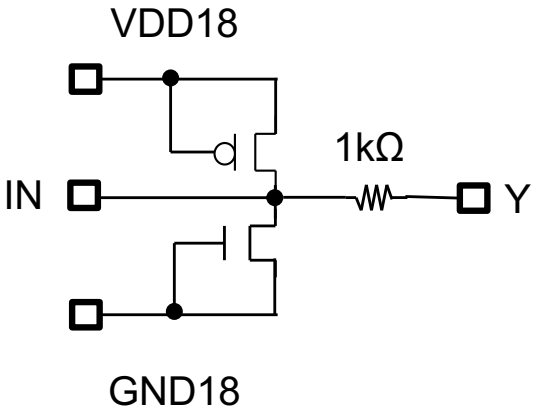
Schematic



4. I/O Buffer cells

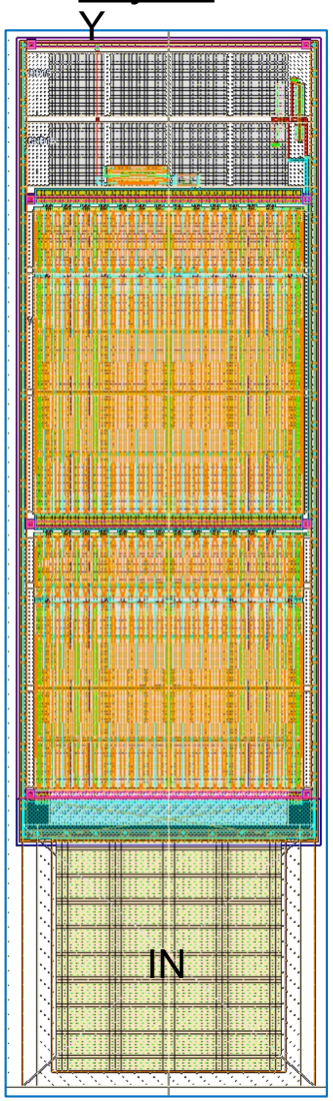
4-9. iodr_5M4_1P8 (Analog pad with protection diodes and resistor)

Logic Symbol

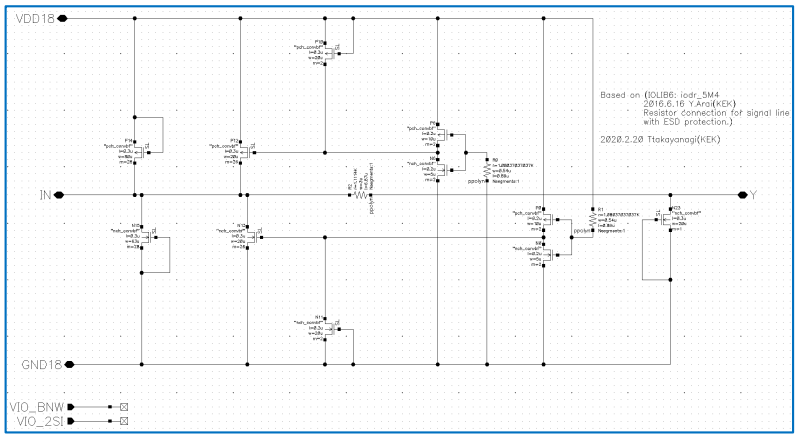


Use this cell for voltage signal, which should be protected from external noise, between VSS and VDD18.

Layout



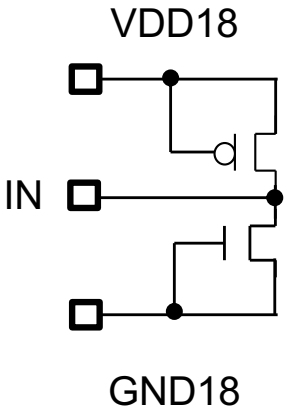
Schematic



4. I/O Buffer cells

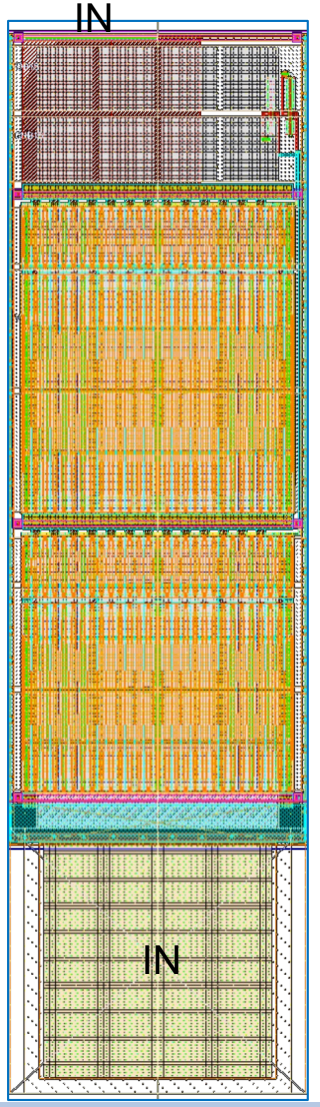
4-10. iod_5M4_1P8 (Analog pad with protection diodes)

Logic Symbol

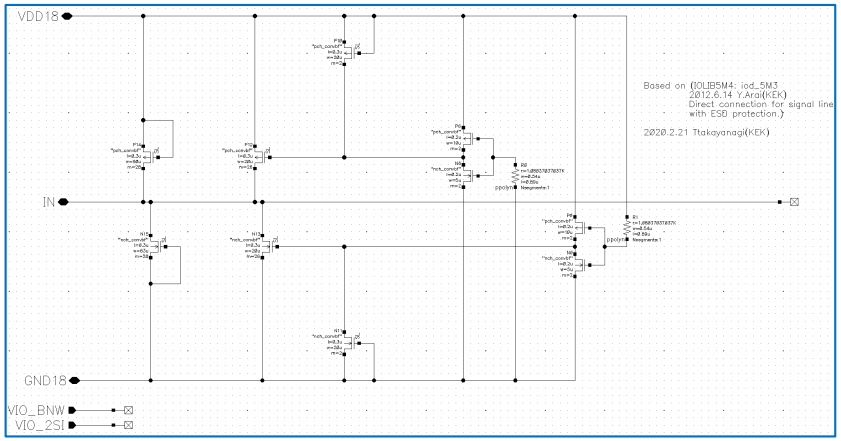


Use this cell for voltage or current supply between VSS and VDD18.

Layout



Schematic



4. I/O Buffer cells

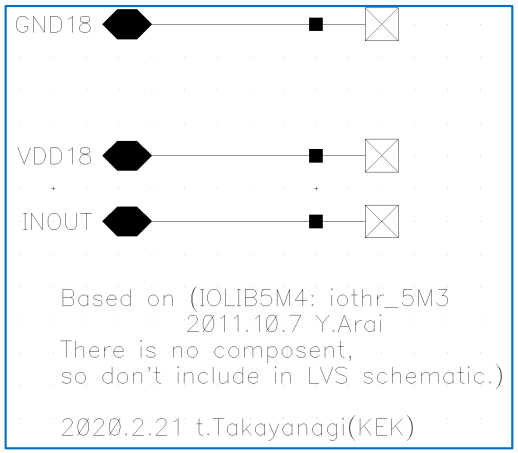
4-11. iothr_5M4_1P8 (Direct analog pad)

Logic Symbol

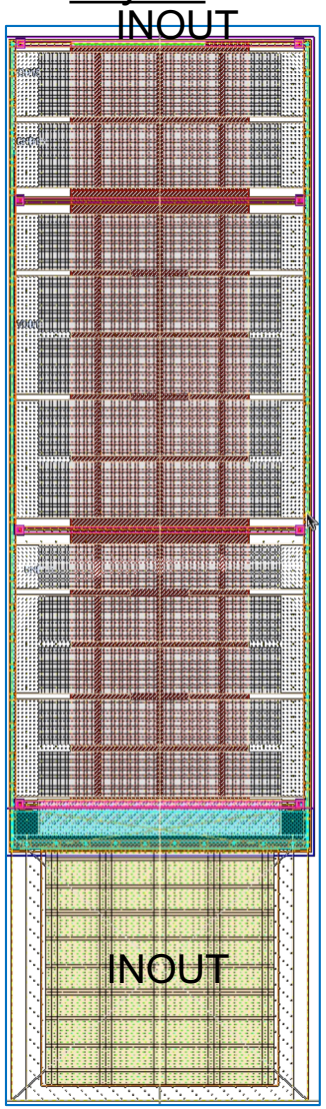
INOUT ☐

Use this cell for voltage outside of VSS~VDD18, or any signal which must be directly connected to internal circuit without protection circuit.

Schematic



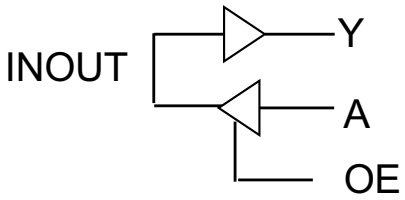
Layout



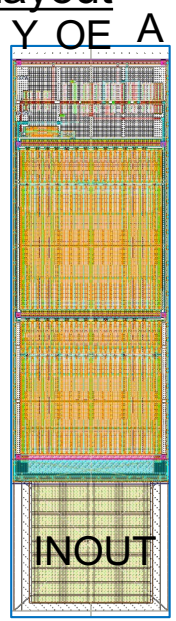
4. I/O Buffer cells

4-12. iobuf_5M4_1P8 (Digital bidirectional Input/Output (4mA) Buffer)

Logic Symbol



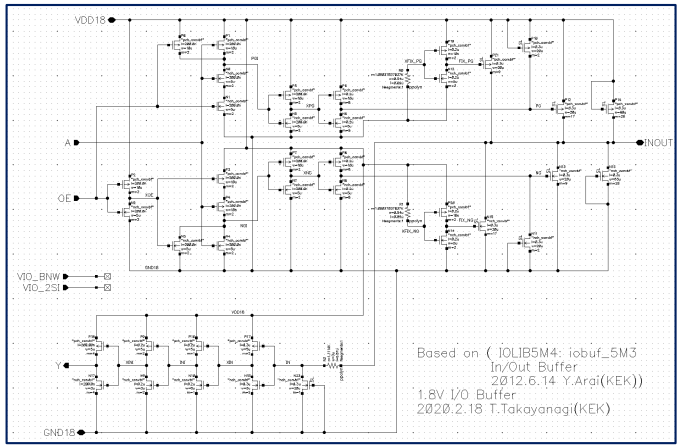
Layout



Truth Table

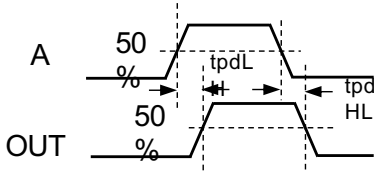
Input A	OE	Output Y	INOUT	
X	0	-	HiZ	High Z
0	1	0	0	Output mode
1	1	1	1	
-	0	0	0	Input mode
-	0	1	1	

Schematic



Delay (c+cc post Simulation Result)

From	To	Tpd	Tpd(ns)
A	INOUT	LH	0.79
		HL	1.33
INOUT	Y	LH	0.35
		HL	0.43



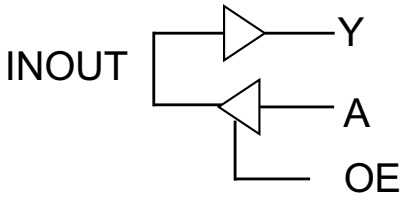
<output Condition> Tr:Typical, VDD18=1.8V, Tj=25deg, F=60MHz, Cload= 25pF

<input Condition> Tr:Typical, VDD18=1.8V, Tj=25deg, F=100MHz, Cload= 0.4pF, OE=L

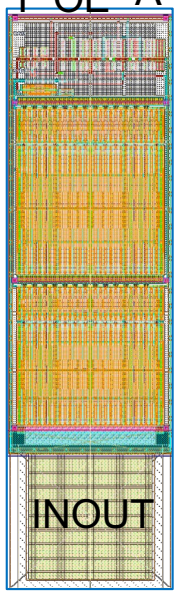
4. I/O Buffer cells

4-13. iobuf2_5M4_1P8 (Digital bidirectional Input/Output (4mA) Buffer with fast return path from A to Y)

Logic Symbol



Layout



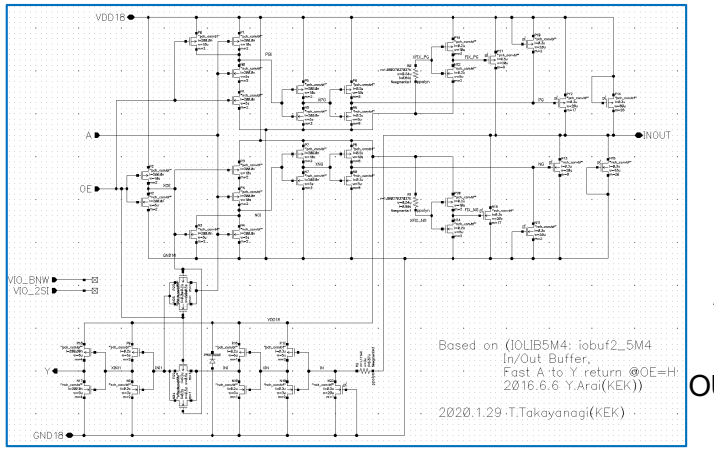
Truth Table

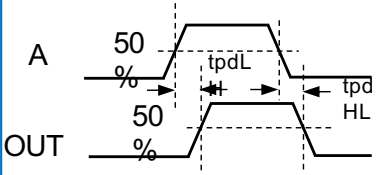
Input A	OE	Output Y	INOUT	
X	0	-	HiZ	High Z
0	1	0	0	Output mode
1	1	1	1	
-	0	0	0	Input mode
-	0	1	1	

Delay (c+cc post Simulation Result)

From	To	Tpd	Tpd(ns)
A	INOUT	LH	0.79
		HL	1.33
A	Y	LH	0.42
		HL	0.45

Schematic





<output Condition> Tr:Typical, VDD18=1.8V, Tj=25deg, F=60MHz, Cload= 25pF

<input Condition> Tr:Typical, VDD18=1.8V, Tj=25deg, F=100MHz, Cload= 0.4pF, OE=H

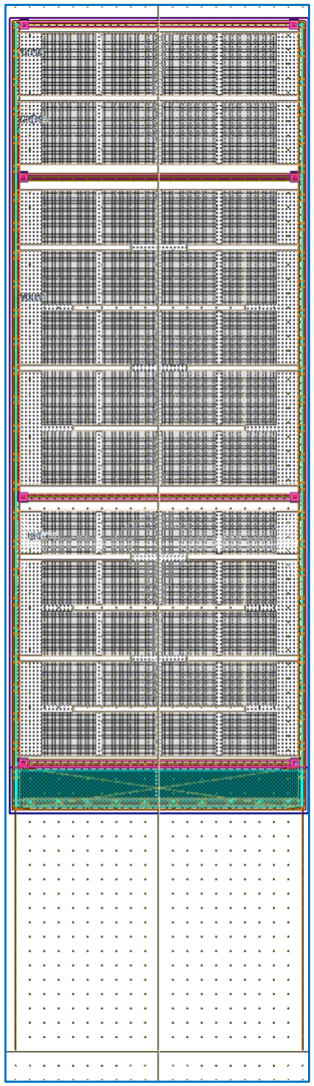
4. I/O Buffer cells

4-14. iofill_5M4_1P8 (IO ring fill cell)

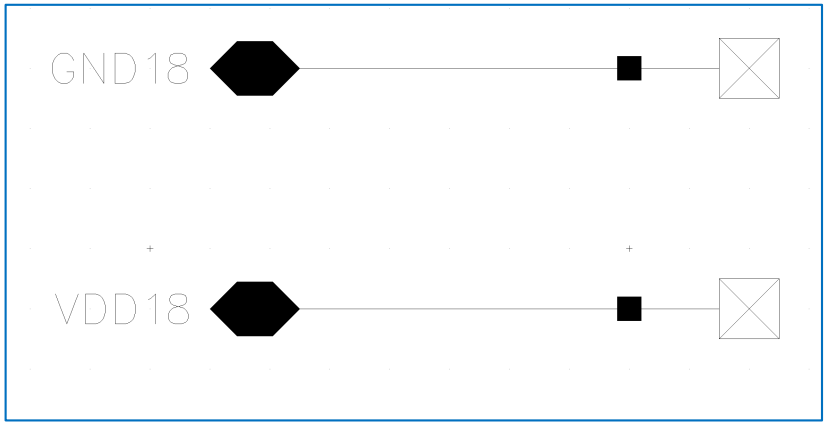
Logic Symbol

This cell is used for Power/GND connection in the I/O ring without pad.

Layout



Schematic



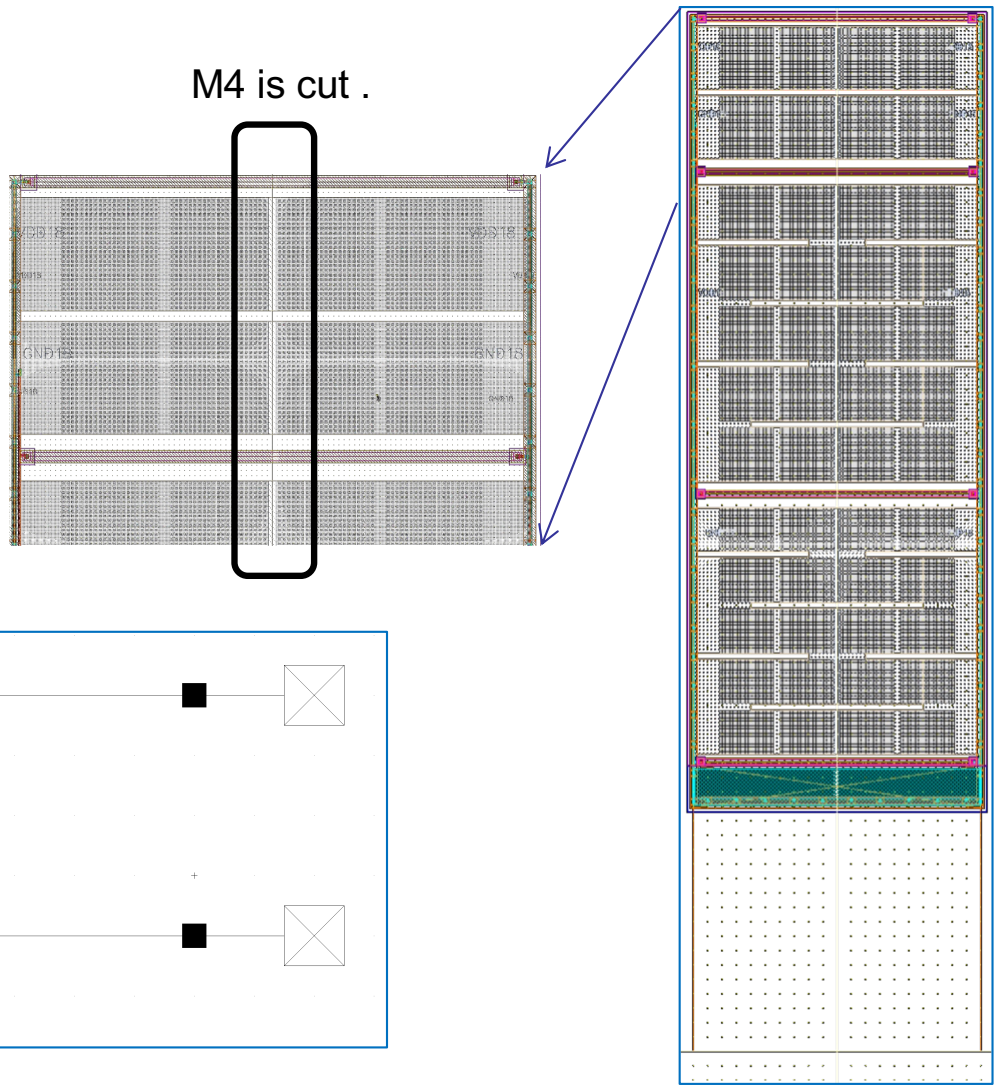
4. I/O Buffer cells

4-15. iofill_M4cut_1P8 (IO ring fill cell. Layer change in M4 power line)

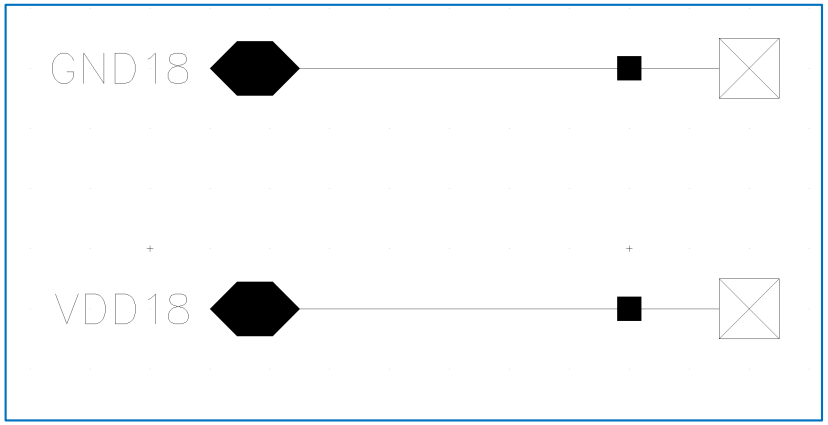
Logic Symbol

There is maximum area DRC rule in Metal 1~4. This cell can be used to cut metal 4 layer in the I/O ring.

Layout



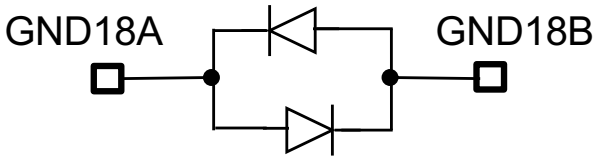
Schematic



4. I/O Buffer cells

4-16. ioGND2GND_1P8 (bidirectional diode for divided GND)

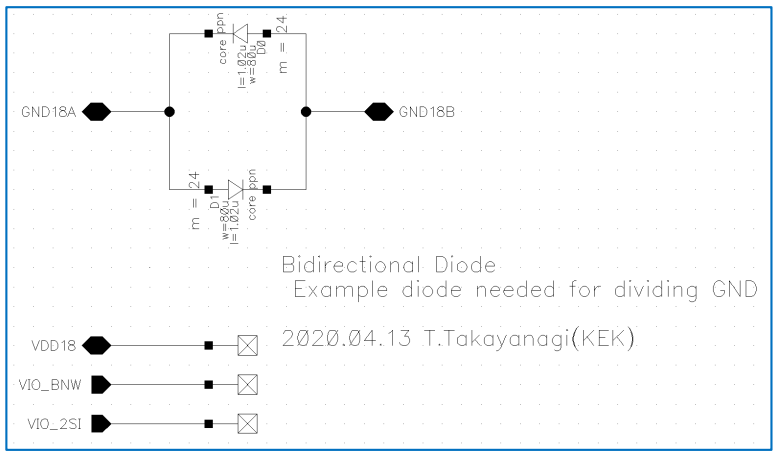
Logic Symbol



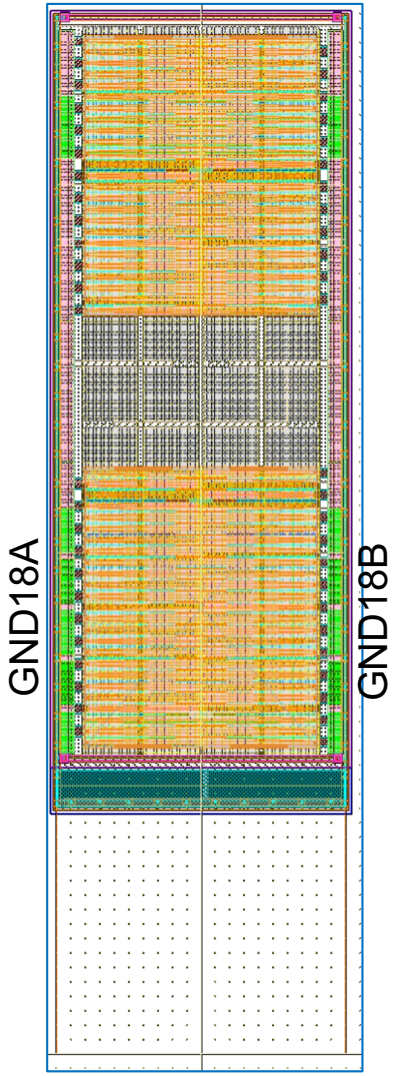
In case of dividing GND , such as analog and digital, it is needed to insert bidirectional diode between all GND for keeping ESD performance.

This cell is just a example , number of diode stage should be determined in each device .

Example Schematic



Example Layout



5. Analog Buffer cells

5-1. Analog Buffers

1.8V IOLIB(IOLIBP1_1P8)のAnalog Bufferに、新たに2種類のBufferを加えた。それぞれのBufferの特徴を下表に、また特性を次ページ以降に示す。

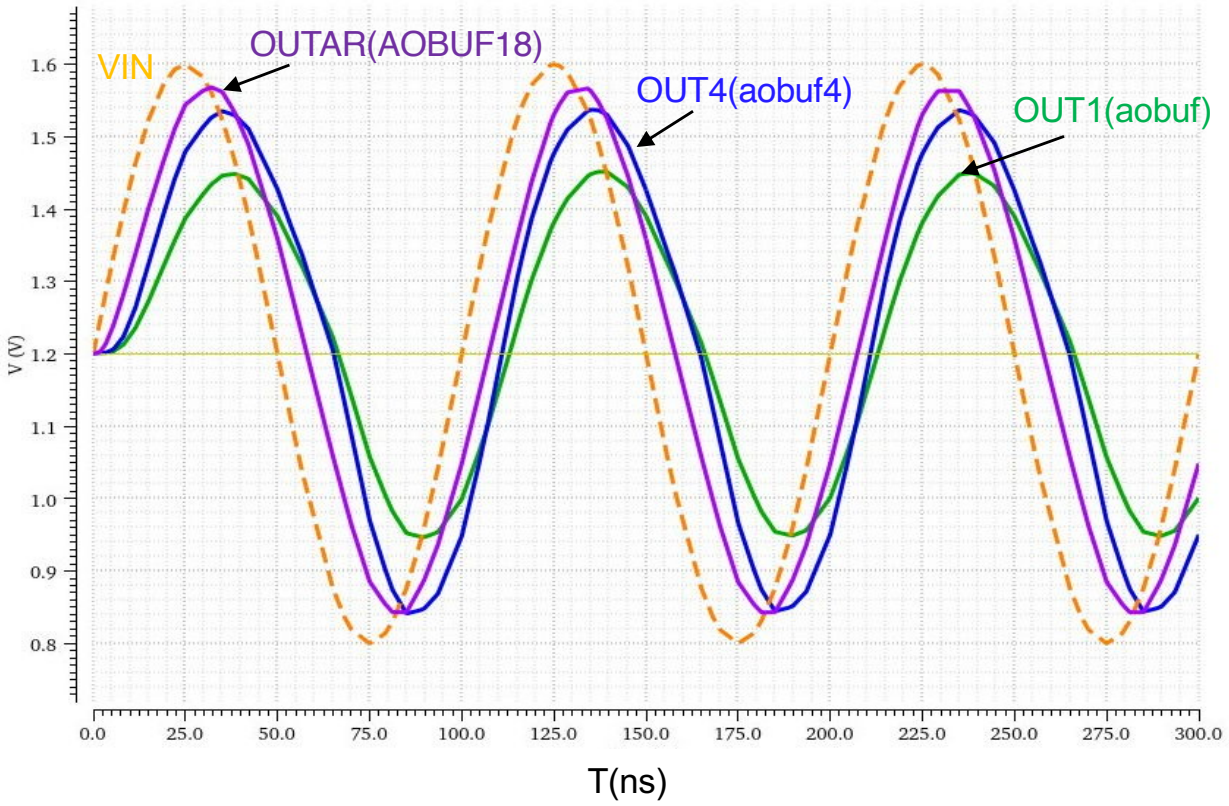
I/O Cell Name	Bias Cell Name	ESD耐性	Linearity/ Drive能力	Comment
io_aobuf_1P8	ioBIAS18_5M4_RR	◎	△	初期バージョン IO Pad領域に置ける （高さ~150um超過）
io_aobuf4_1P8	ioBIAS18_5M4_RR	○	○	Io_aobuf_1P8互換。 出力抵抗削除。 Transfer Gate増強。
Io_aobufar_1P8	ARO_BIAS18_AOB04AB	△	◎	A-R-Tec社製作。 内部Core Tr使用

5. Analog Buffer cells

5-1. Analog Buffers

Transition Simulation

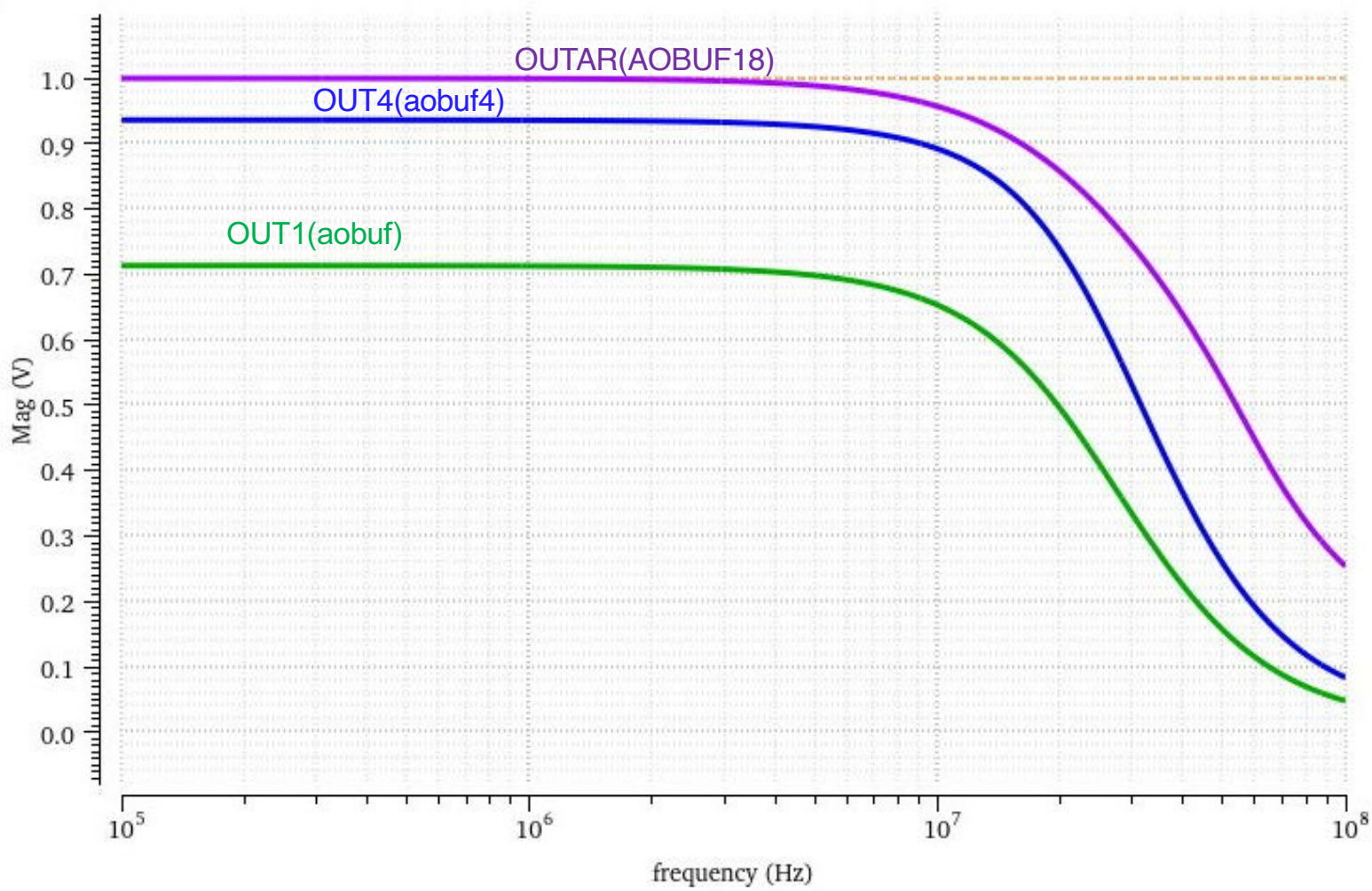
SEABAS2/3相当の負荷(1kΩ+10pF, 1.2V終端) 時の、10MHzサイン波に対する出力波形の比較を示す。
従来型のio_aobuf_1P8では入力より約40%振幅が減少するが、改良型のio_aobuf4_1P8では約15%減少。
また、A-R-Tec製作のBuffer では約10%の減少であった。



5. Analog Buffer cells

5-1. Analog Buffers

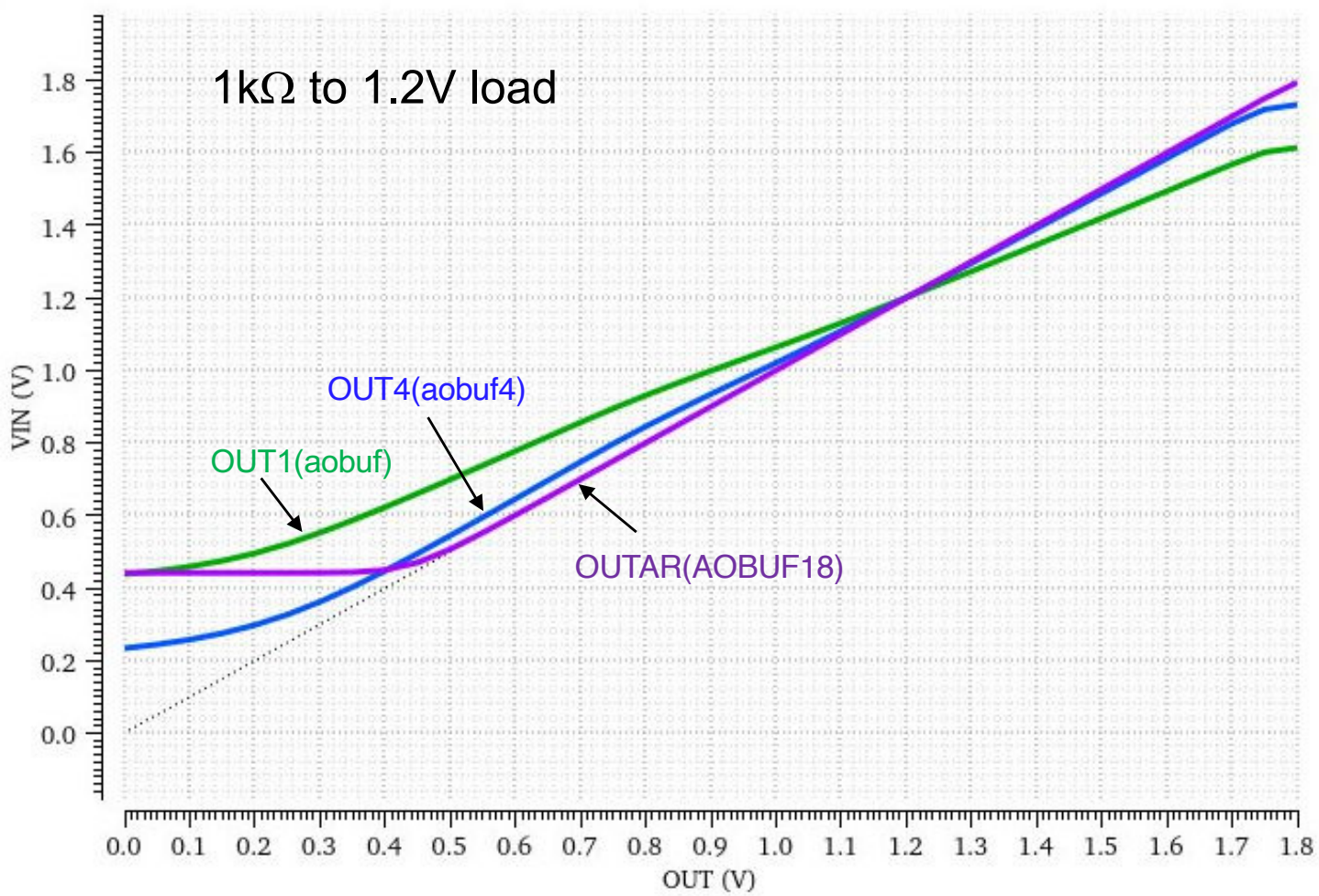
AC Simulation



5. Analog Buffer cells

5-1. Analog Buffers

DC Simulation

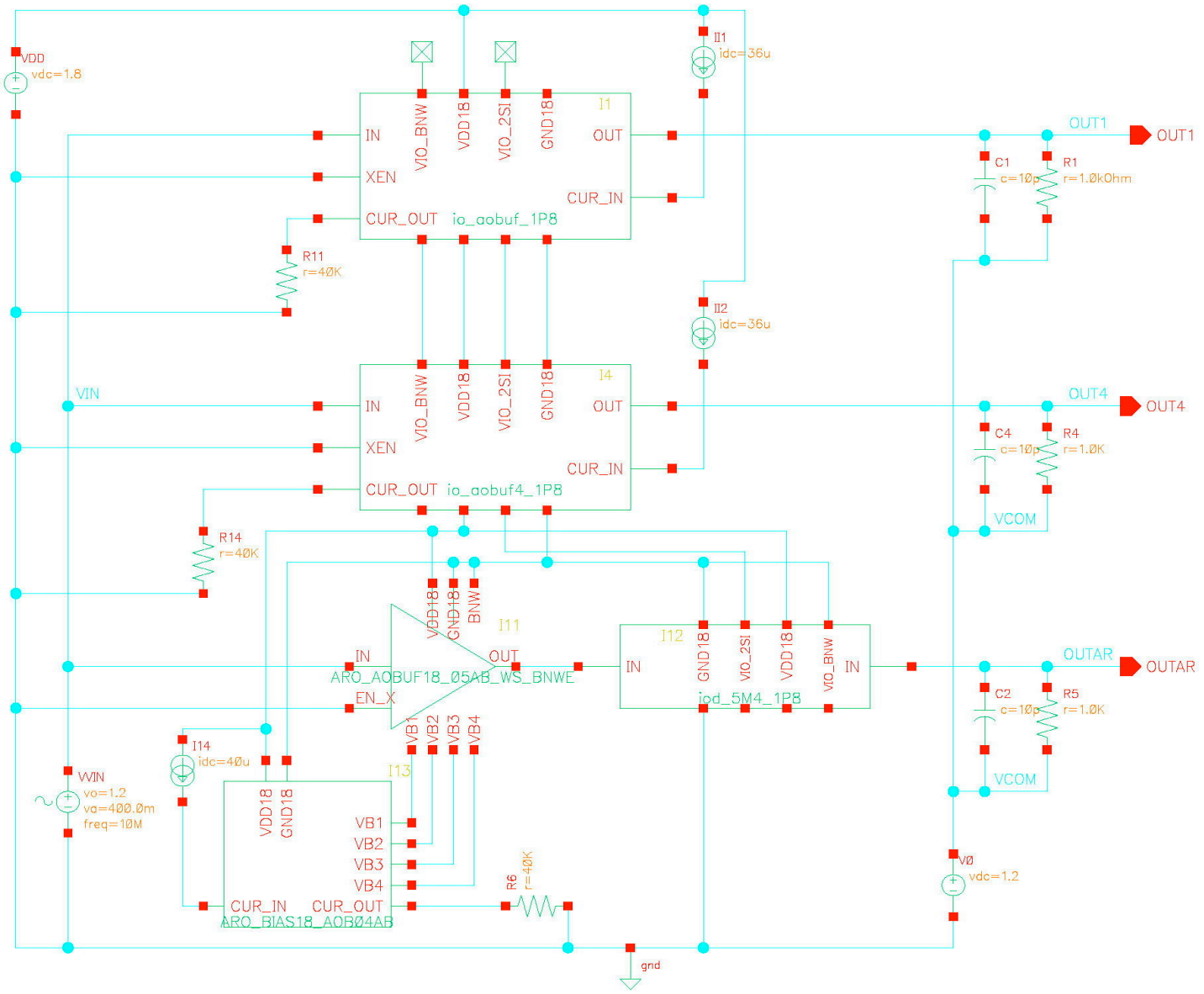


AOBUF18(io_aobufar_1P8)が最も線型性が良い。

5. Analog Buffer cells

5-1. Introduction

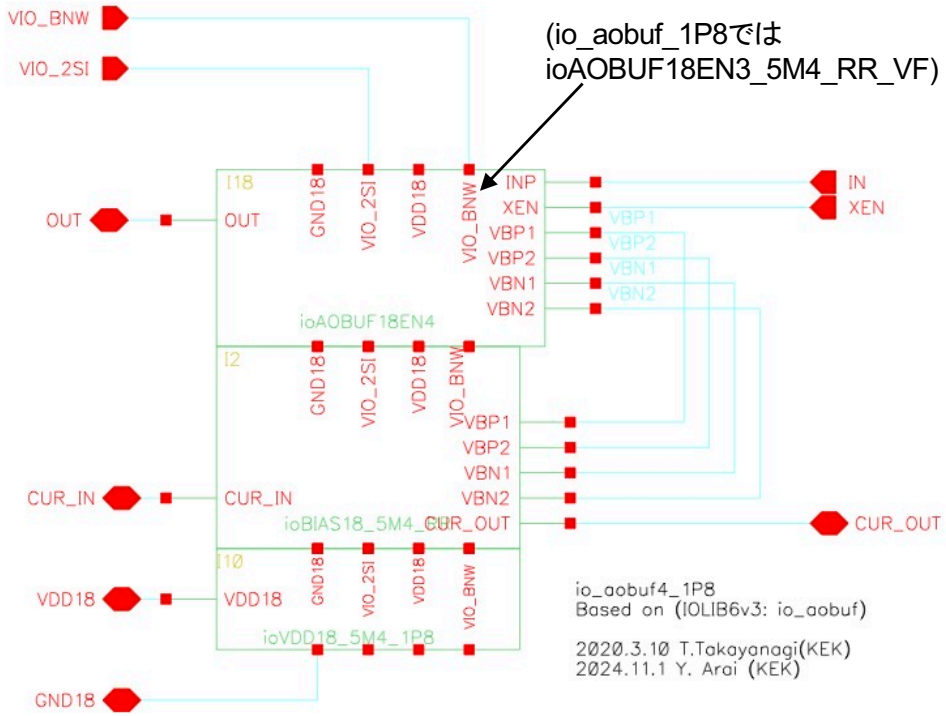
Simulation回路



5. Analog Buffer cells

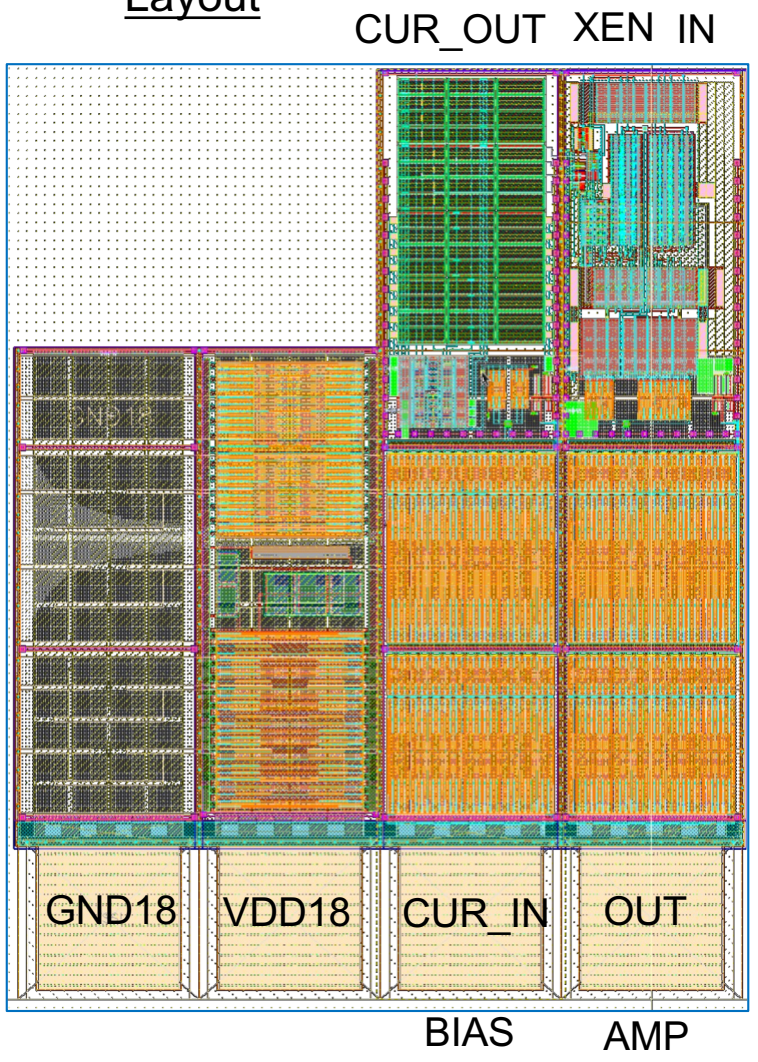
5-2. io_aobuf4_1P8 & io_aobuf_1P8 (Schematic & layout example)

Schematic



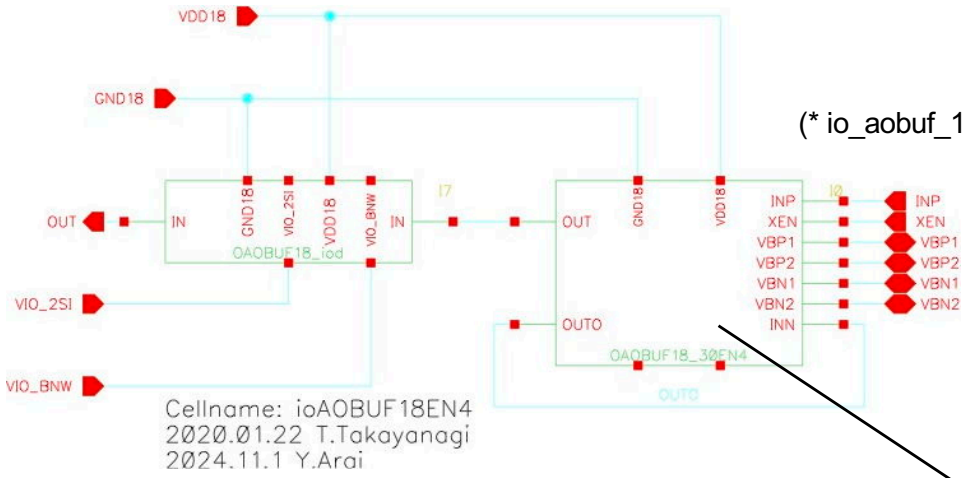
CUR_INの標準値は36uAでこの時V(CUR_IN)=0.73V
XEN=Lで出力Enable.

Layout



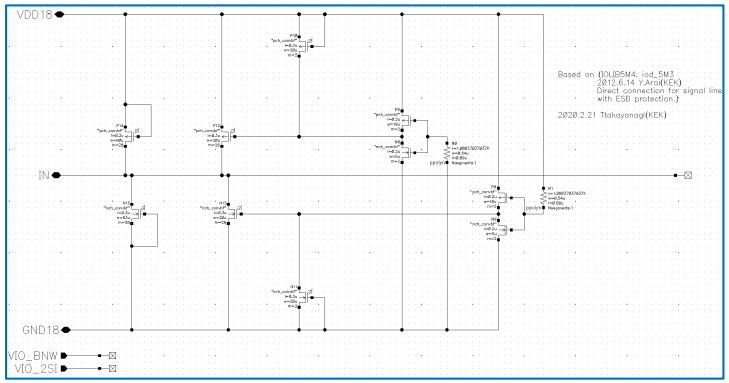
5. Analog Buffer cells

5-2. io_aobuf4_1P8 & io_aobuf_1P8 (Schematic2)



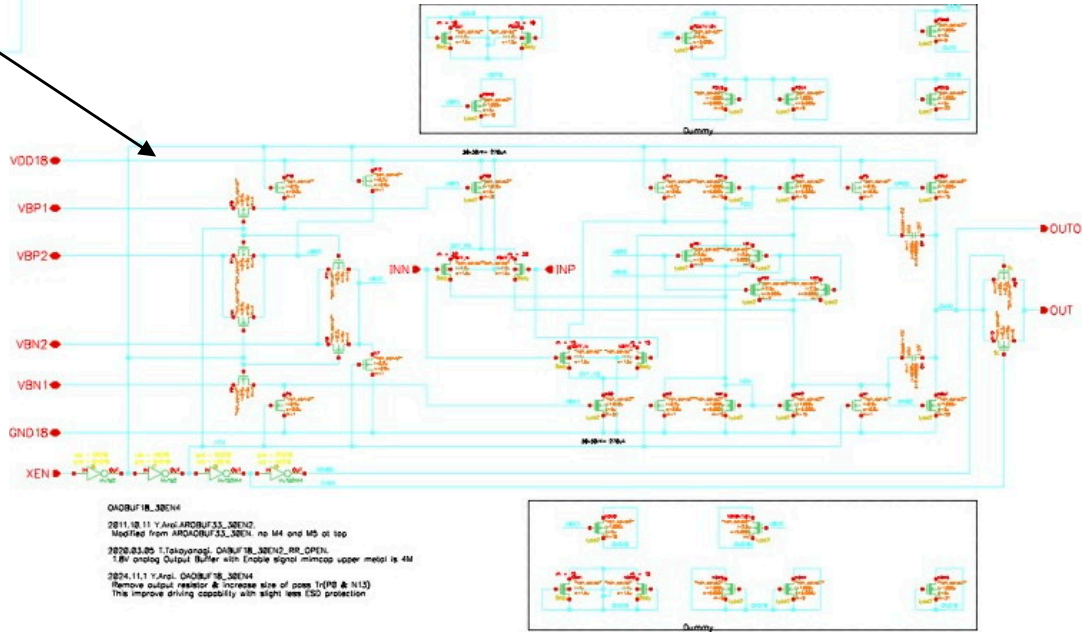
(* io_aobuf_1P8では ioAOBUF18EN3_5M4_RR_VF)

PAD schematic



iod_5M4_1P8

AMP schematic

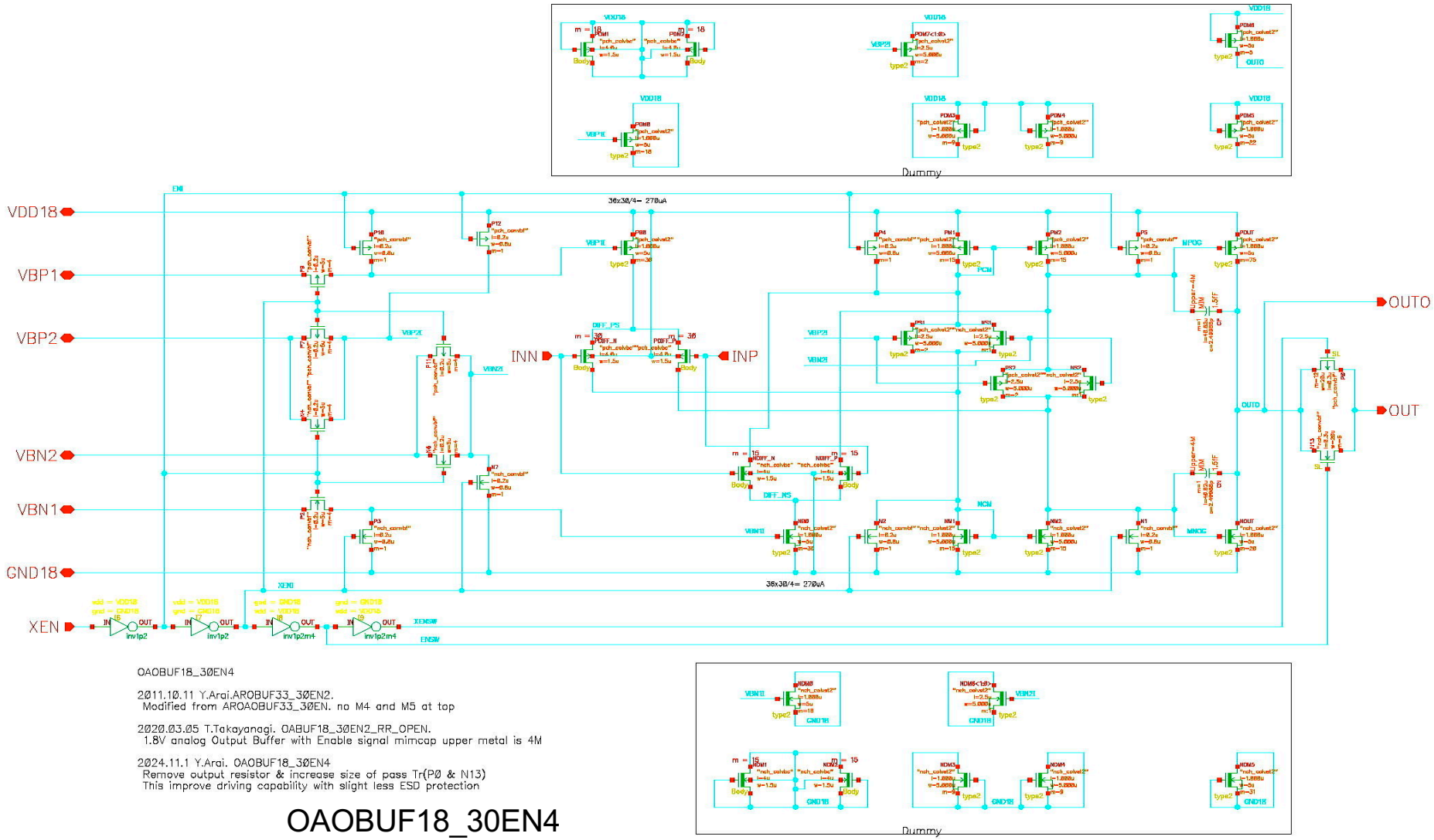


OAOBUF18_30EN4

(* io_aobuf_1P8では OAOBUF18_30EN2_RR_OPEN)

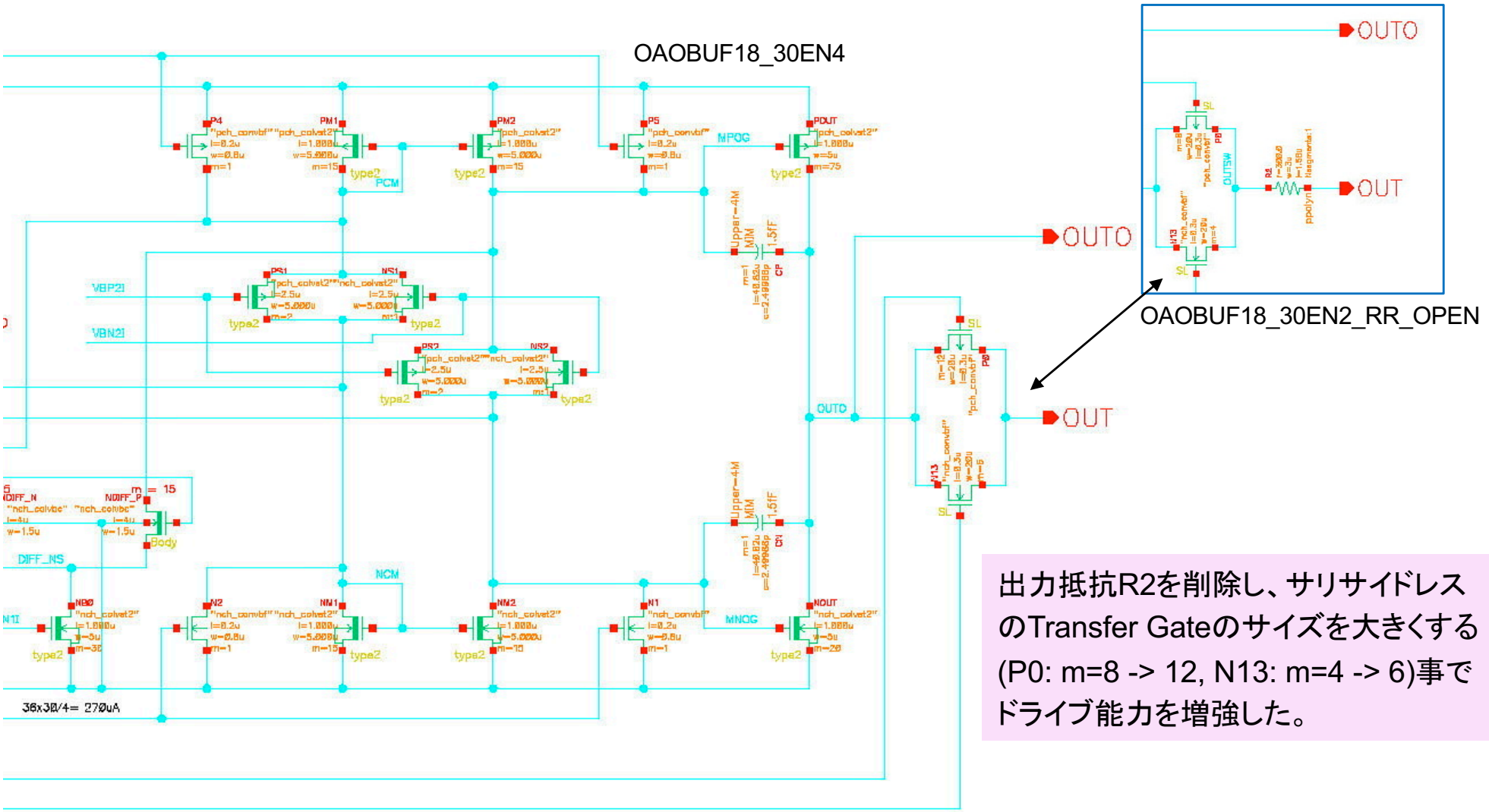
5. Analog Buffer cells

5-2. io_aobuf4_1P8 & io_aobuf_1P8 (Schematic3)



5. Analog Buffer cells

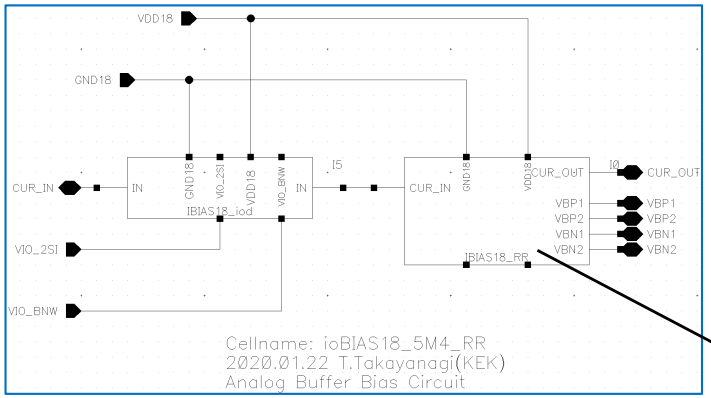
5-2. io_aobuf4_1P8 & io_aobuf_1P8 (Schematic4, Difference)



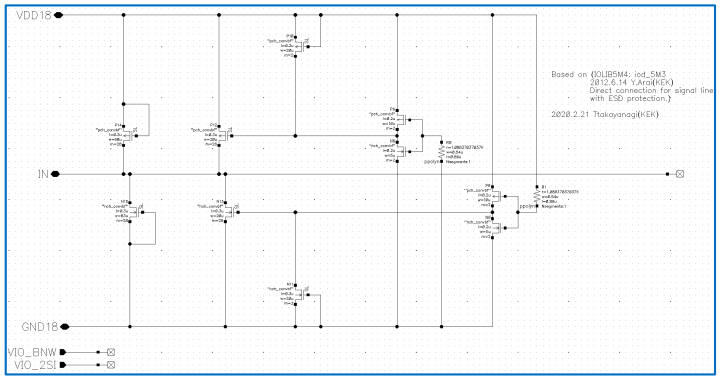
出力抵抗R2を削除し、サリサイドレスのTransfer Gateのサイズを大きくする(P0: m=8 -> 12, N13: m=4 -> 6)事でドライブ能力を増強した。

5. Analog Buffer cells

5-2. io_aobuf4_1P8 & io_aobuf_1P8 (Schematic5, Bias circuit)

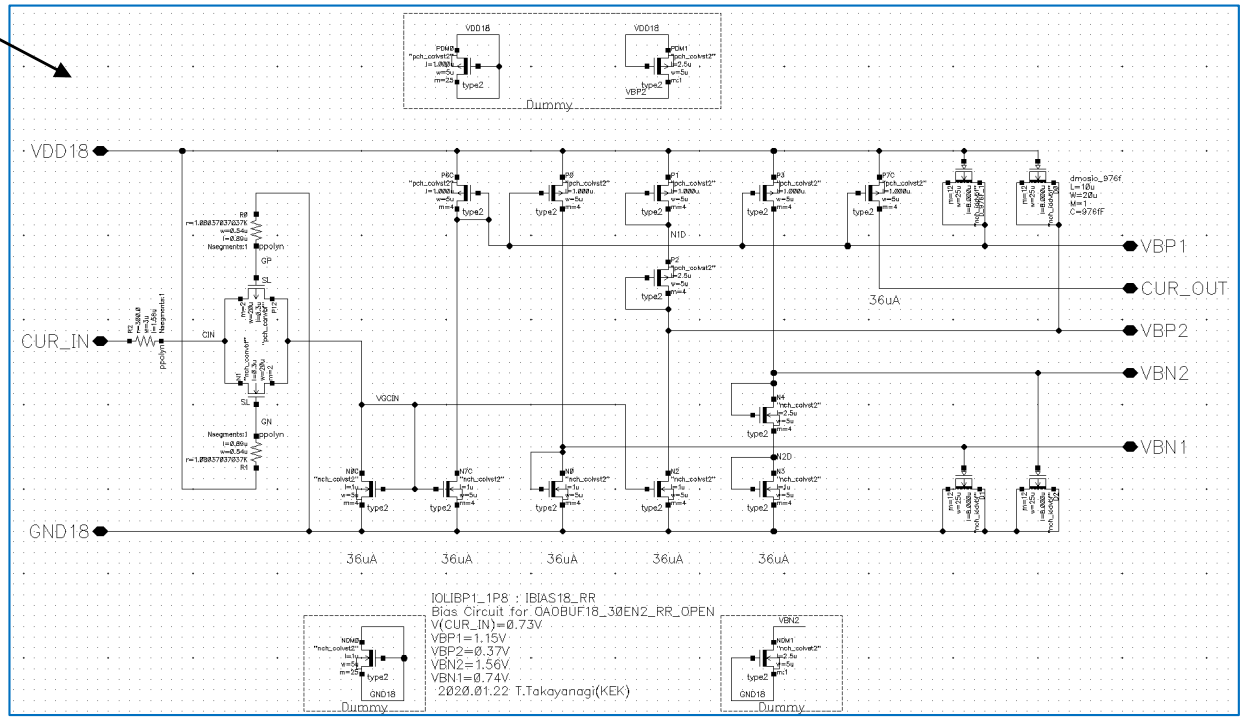


PAD schematic



iod_5M4_1P8

BIAS schematic



IBIAS18_RR

5. Analog Buffer cells

5-2. io_aobuf_1P8 (Specification)

Characteristic

Netlist AMP→ post netlist / R+C+CC mode
BIAS→ post netlist / C+CC mode

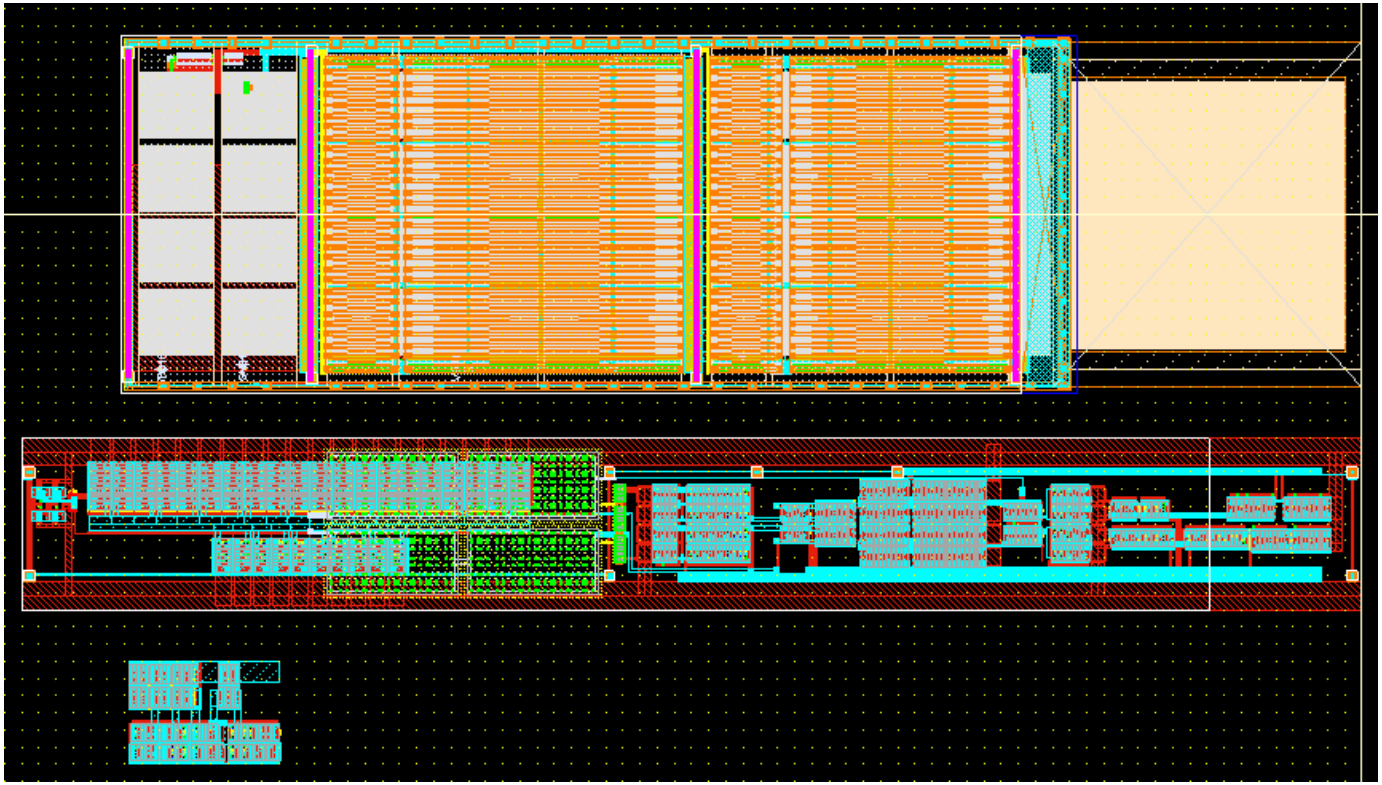
項目		3.3V版 仕様書 Min	Typ	Max	Hspice Min	Typ	Max	単位	判定	補足	1.8V版 仕様書 Min	Typ	Max	Hspice Min	Typ	Max	単位	判定	補足
電源電圧			**3.3**		3.0	3.3	3.6	V	○			**1.8**		1.65	**1.8**	1.95	V	○	
電源電流	平均値		**2000**		2162	2279	2426	uA	○	T=25°C		**2000**		264.3	**522.7**	709.1	uA	○	@IBIAS=36μA,VIN=0.9V
負荷抵抗			**1.0**		2			kΩ	△								kΩ		
負荷容量			**20**			20		pF	△			**20**			**20**		pF		
入出力電圧範囲					0.40		2.00	V						0.20		1.60	V		
VDD=3.3V	min		**0.4**			0.20	0.45					**0.2**			**0.2**				VDD=1.8V
	max		**2.2**		2.05	2.30						**1.6**			**1.6**				
VDD=3.0V	min					0.20	0.45								-				
	max				2.00	2.10									-				
ユニティゲインバッファAC特性																			
DCゲイン	@1KHz		**0.0**		-0.01	0.00	0.10	dB	○			**0.0**			**0.00**		dB	○	
帯域（BW）	f(-3dB)		**40**		29.7	59.1	159.9	MHz	△	in=0.4~2.2V				4.324	**10.62**	17.5	MHz		in=0.2~1.6V
			40		41.3	63.1	159.9		○	in=0.4~2.0V				-	-	-			
入力換算雑音	Vni				38	43	69	uV						43.6	**58.6**	130.9	uV		BWまで積分
オープンループAC特性																			
DCゲイン	@1KHz				47	63	68	dB						11	**76**	79	dB		
ユニティゲイン周波数	fu				20.4	36.3	84.8	MHz		in=0.4~2.2V				2.4	**13.2**	20.9	MHz		in=0.2~1.6V
					27.4	38.5	71.2			in=0.4~2.0V				-	-	-			
位相余裕	PM		**60**		56.9	64.5	81.0	deg	△	CL=20pF		**60**		62.6	**67.2**	91.4	deg	○	CL=20pF
					60.3	68.1	84.7		○	CL=17pF				62.6	**66.7**	91.8		○	CL=17pF
ユニティゲインバッファTR特性																			
○入力ステップ電圧＝0.1V										VL/VH=1.15/1.25V									VL/VH=0.85/0.95V
セトリング時間（VL→VH）	99%				4.5	6.1	7.9	ns						58.5	**84.8**	141.4	ns		
	99.9%				8.3	15.6	22.1	ns						74.8	**124.4**	219.1	ns		
セトリング時間（VH→VL）	99%				3.7	5.2	12.9	ns						59.2	**86.5**	150.9	ns		
	99.9%				11.5	15.9	23.7	ns						74.1	**128.0**	231.0	ns		
オーバーシュート	Vo sh				0.3	0.6	10.3	mV						1.9	**3.5**	7.0	mV		
アンダーシュート	Vu sh				0.2	0.3	5.7	mV						1.7	**3.3**	5.9	mV		
○入力ステップ電圧＝0.8V										VL/VH=0.4/2.0V									VL/VH=0.4/1.4V
セトリング時間（VL→VH）	99%				31.8	35.5	39.7	ns						46.5	**80.9**	110.2	ns		
	99.9%				44.4	59.7	82.3	ns						77.5	**97.0**	164.1	ns		
セトリング時間（VH→VL）	99%				15.2	20.6	28.7	ns						49.8	**59.8**	129.8	ns		
	99.9%				46.6	67.5	93.3	ns						90.8	**113.6**	183.6	ns		
オーバーシュート	Vo sh				64.4	112.3	175.1	mV						15.9	**24.0**	61.7	mV		
アンダーシュート	Vu sh				1.4	1.5	1.7	mV						0.6	**7.3**	39.7	mV		
スルーレート	SR				37.1	40.6	45.5	V/us						23.7	**42.2**	73.1	V/us		VIN=0-1.8V, 0.5-1.3V meas
オフセット	OF							mV						0.228	**-0.13**	1.591	mV		VIN=0.9V

Max/Min value are extracted from PVT (Process Voltage Temp) simulation result

5. Analog Buffer cells

5-3. io_aobufar_1P8 (Layout)

Layout



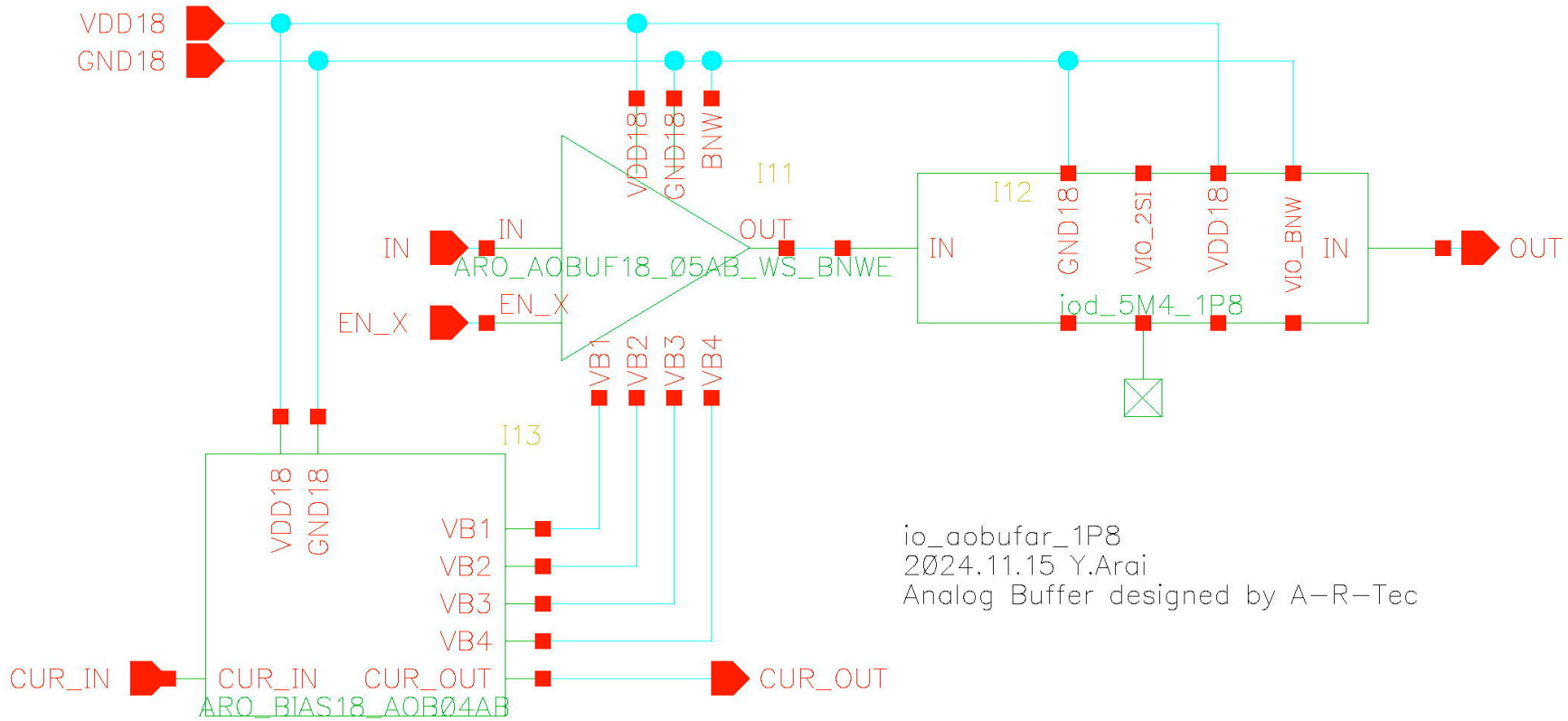
lod_5M4_1P8

ARO_AOBUF18_05AB
_WS_BNWE

ARO_BIAS18_AOB04AB

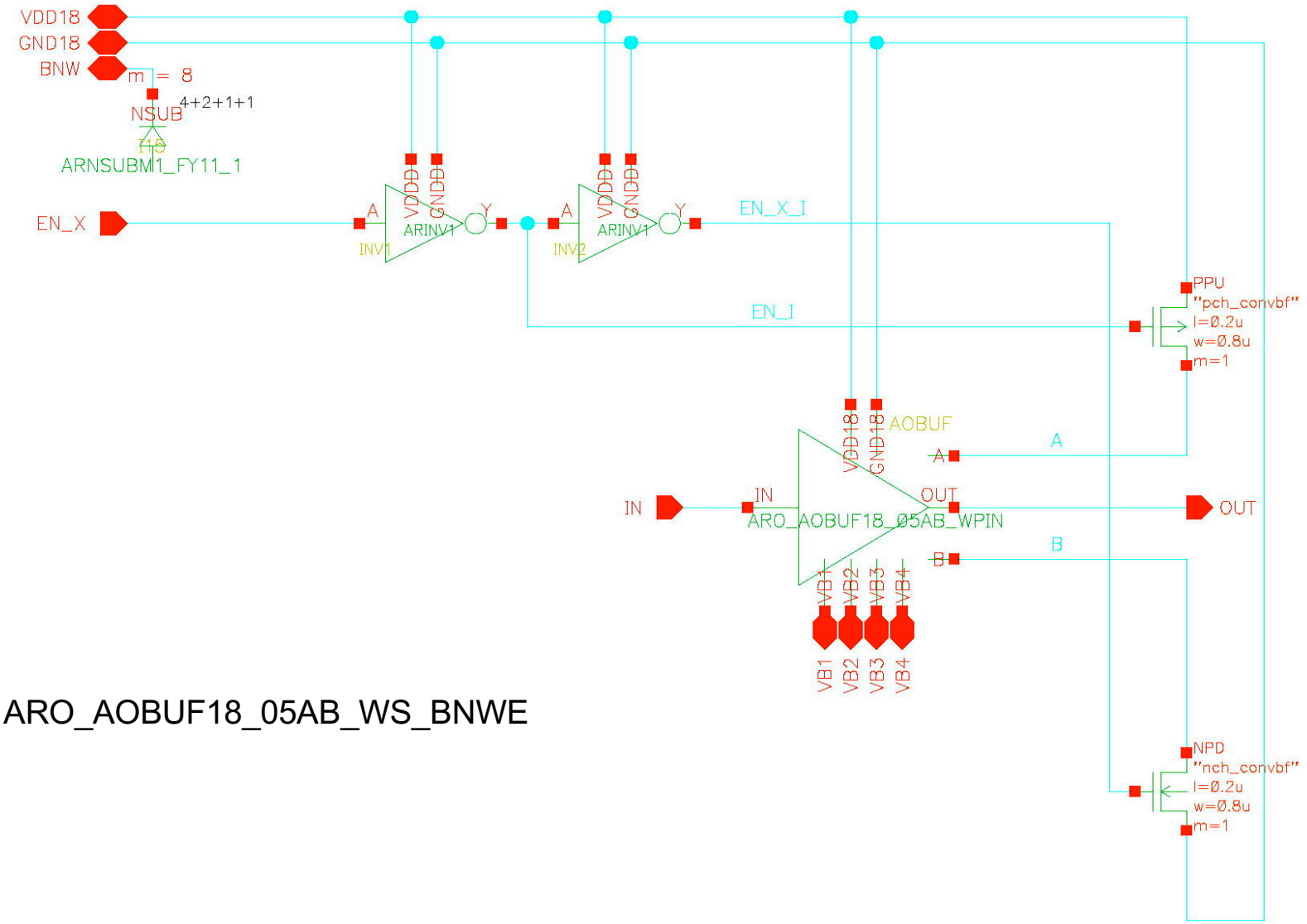
5. Analog Buffer cells

5-3. io_aobufar_1P8 (Schematic1)



5. Analog Buffer cells

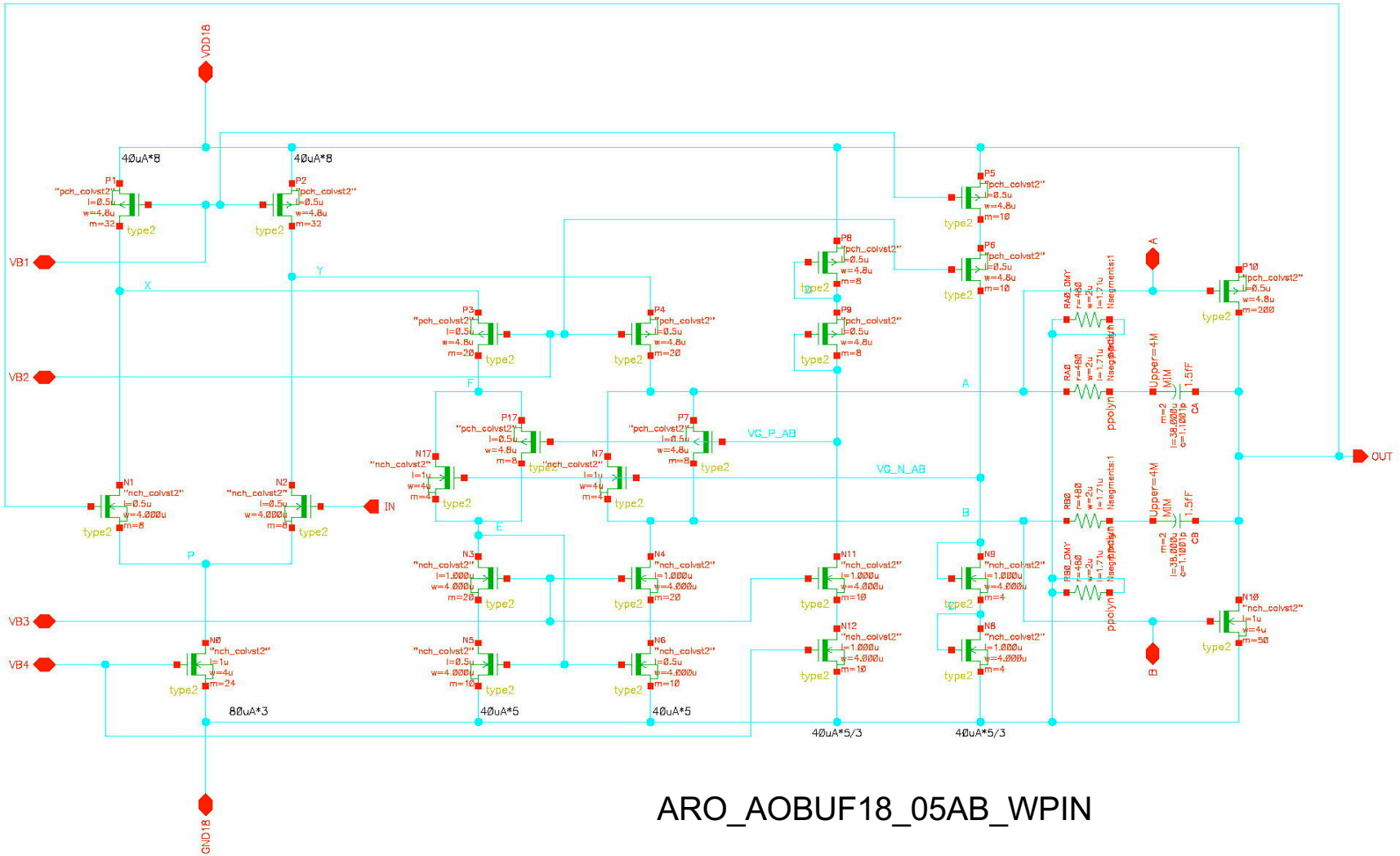
5-3. io_aobufar_1P8 (Schematic2, Amp)



ARO_AOBUF18_05AB_WS_BNWE

5. Analog Buffer cells

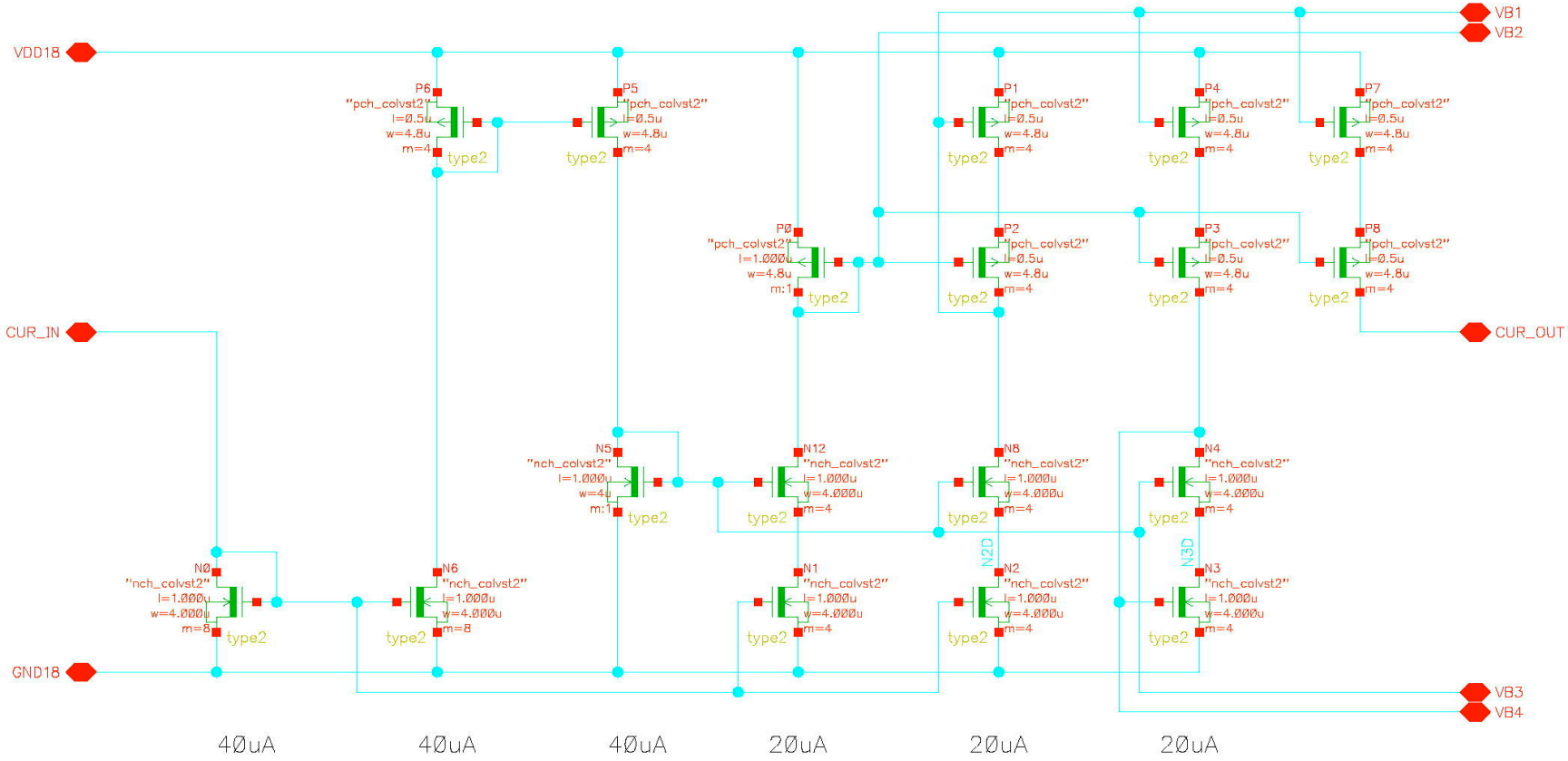
5-3. io_aobufar_1P8 (Schematic3, Amp)



ARO_AOBUF18_05AB_WPIN

5. Analog Buffer cells

5-3. io_aobufar_1P8 (Schematic4, Bias)



ARO_BIAS18_AOB04AB

6. I/O Buffer rings

6-0. Comment

There are 3 kinds of special pads in 4 corners of iorings.

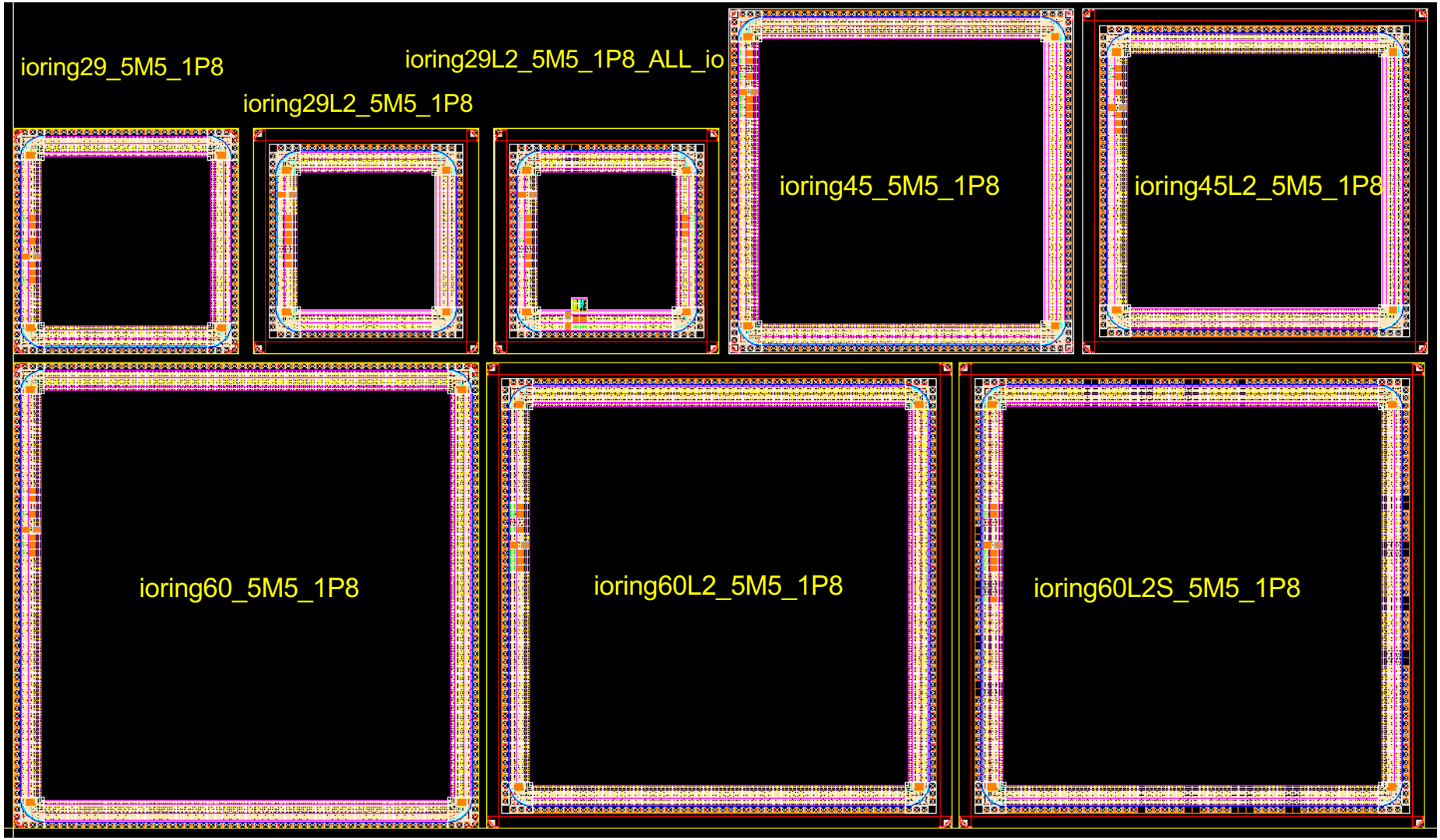
VDET ---- Corner 4 pads which are connected to handle wafer via P+ implant(PSUB).
VIO_BNW --- Connected to BNW ring which covers IO buffers and protect from
back gate problem. Normally this should be connected to ground.
VIO_2SI --- Connection to 2nd SOI layer (2SI or SOI2) which covers IO buffer area.
This pad becomes non-connection in the case of single SOI wafer.

Schematics are same for all 4 examples and shown below. Please replace the IO cells according to your design.

6. I/O Buffer rings

6-1. top_iolib_1P8 (All IO rings)

Layout

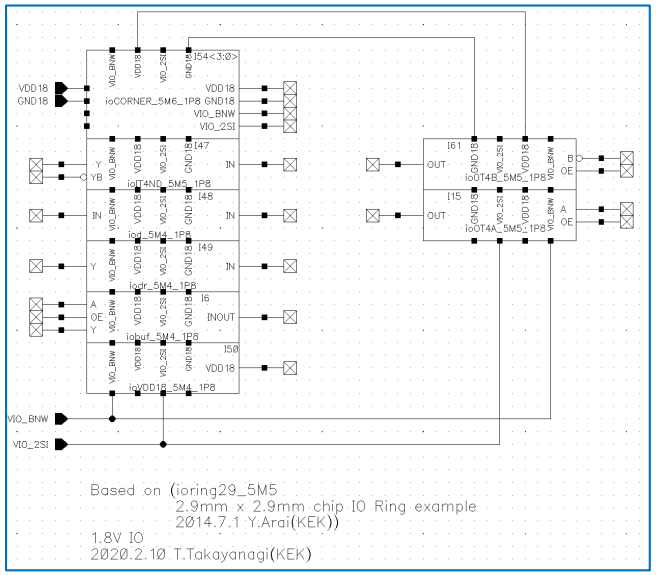


95

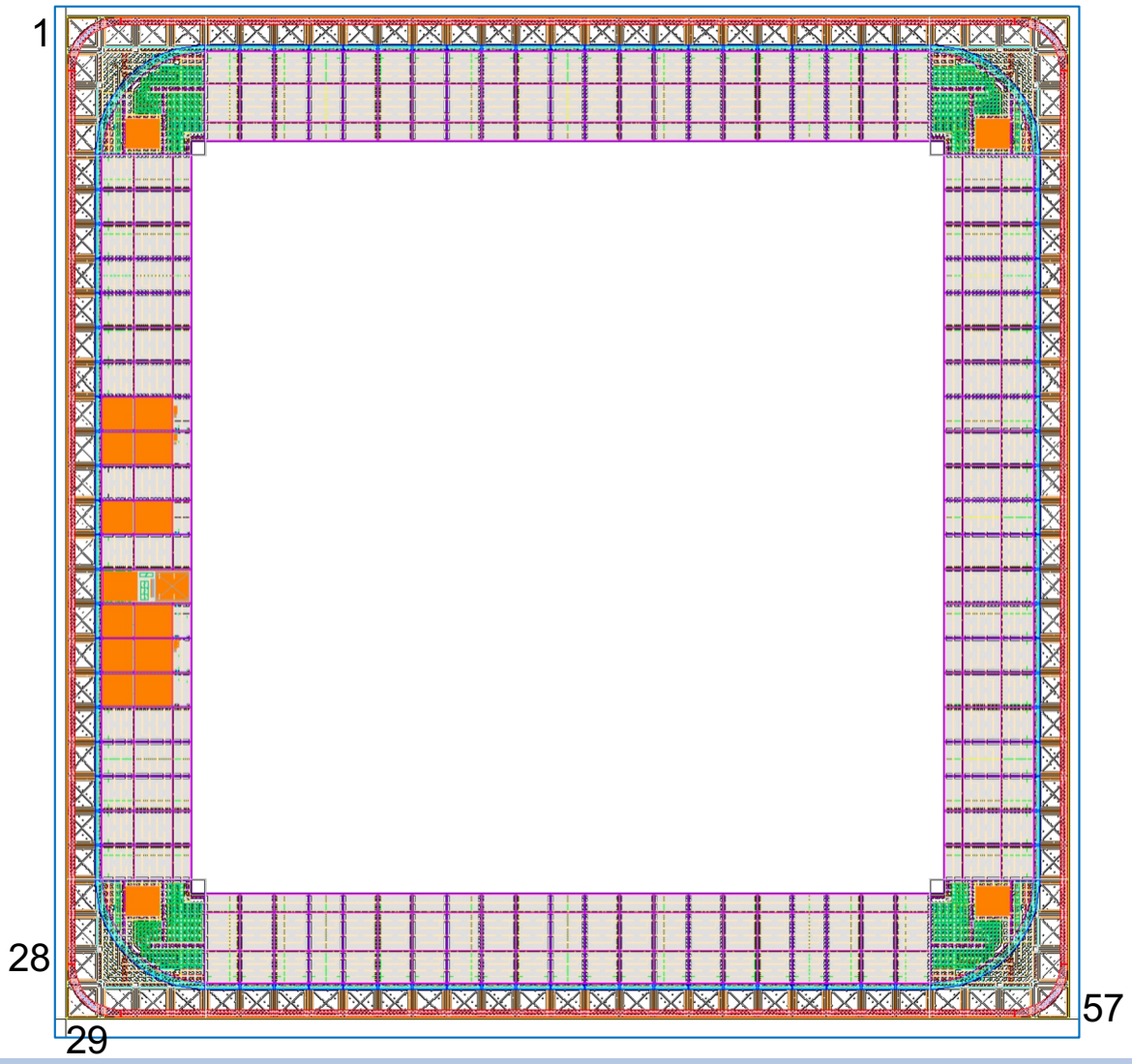
6. I/O Buffer rings

6-2. ioring29_5M5_1P8 (IO ring for 2.9mm chip (PGA178))

Schematic



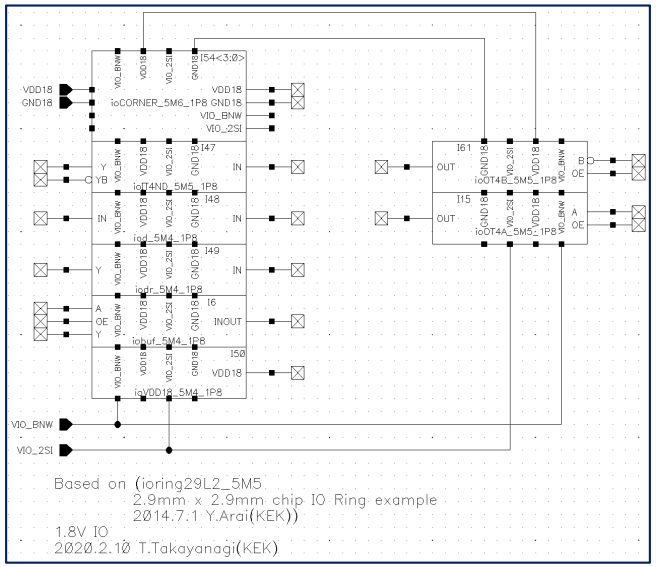
Layout



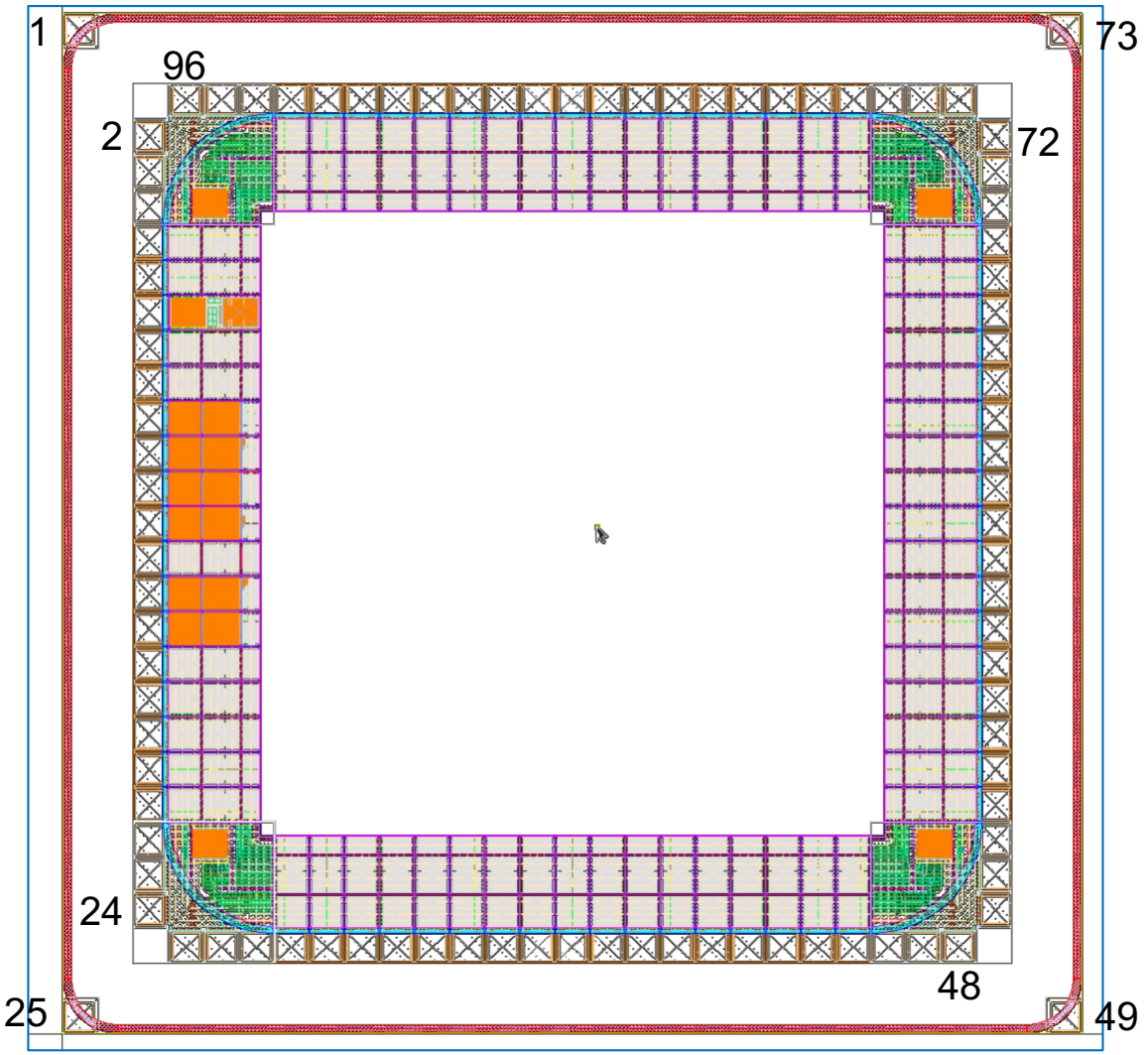
6. I/O Buffer rings

6-3. ioring29L2_5M5_1P8 (IO ring for 2.9mm chip with 200um bias spacing for pixel (PGA178))

Schematic



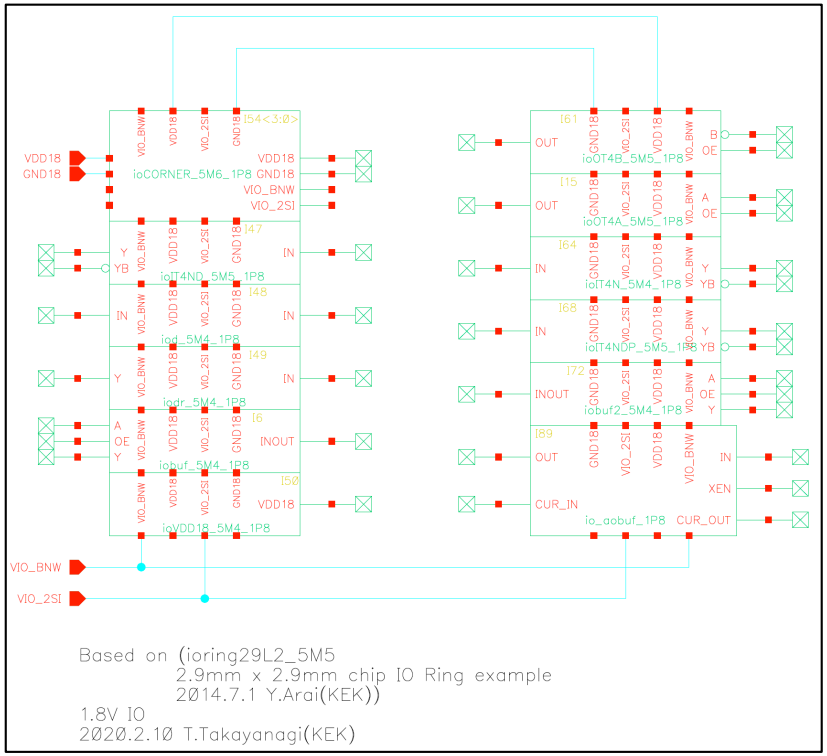
Layout



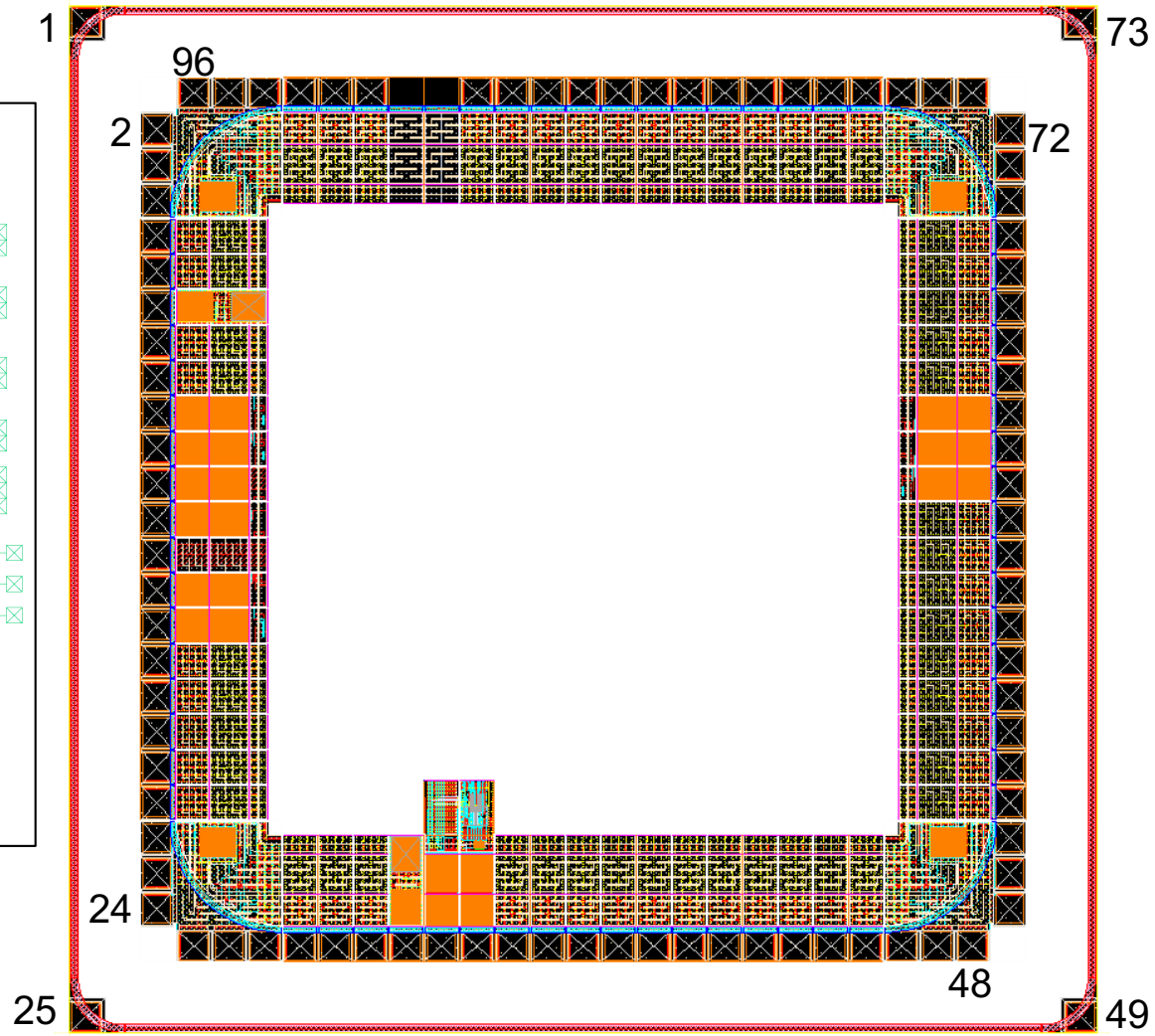
6. I/O Buffer rings

6-4. ioring29L2_5M5_1P8_ALL_io (IO ring for 2.9mm chip with 200um bias spacing for pixel (PGA178), include analog output buffer)

Schematic



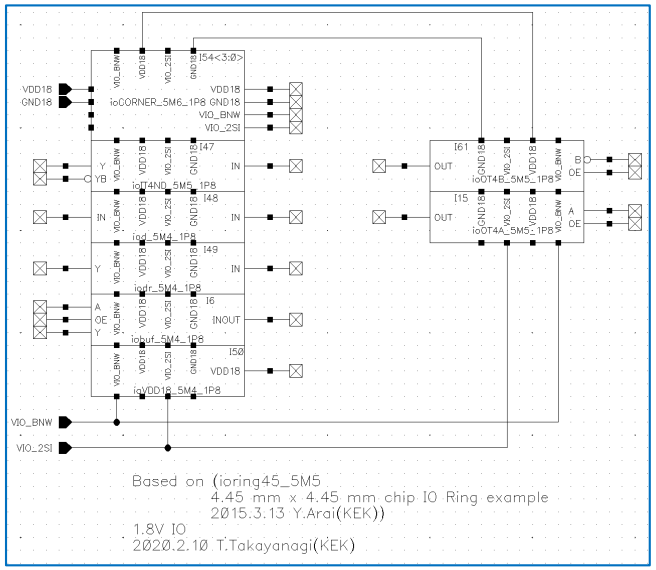
Layout



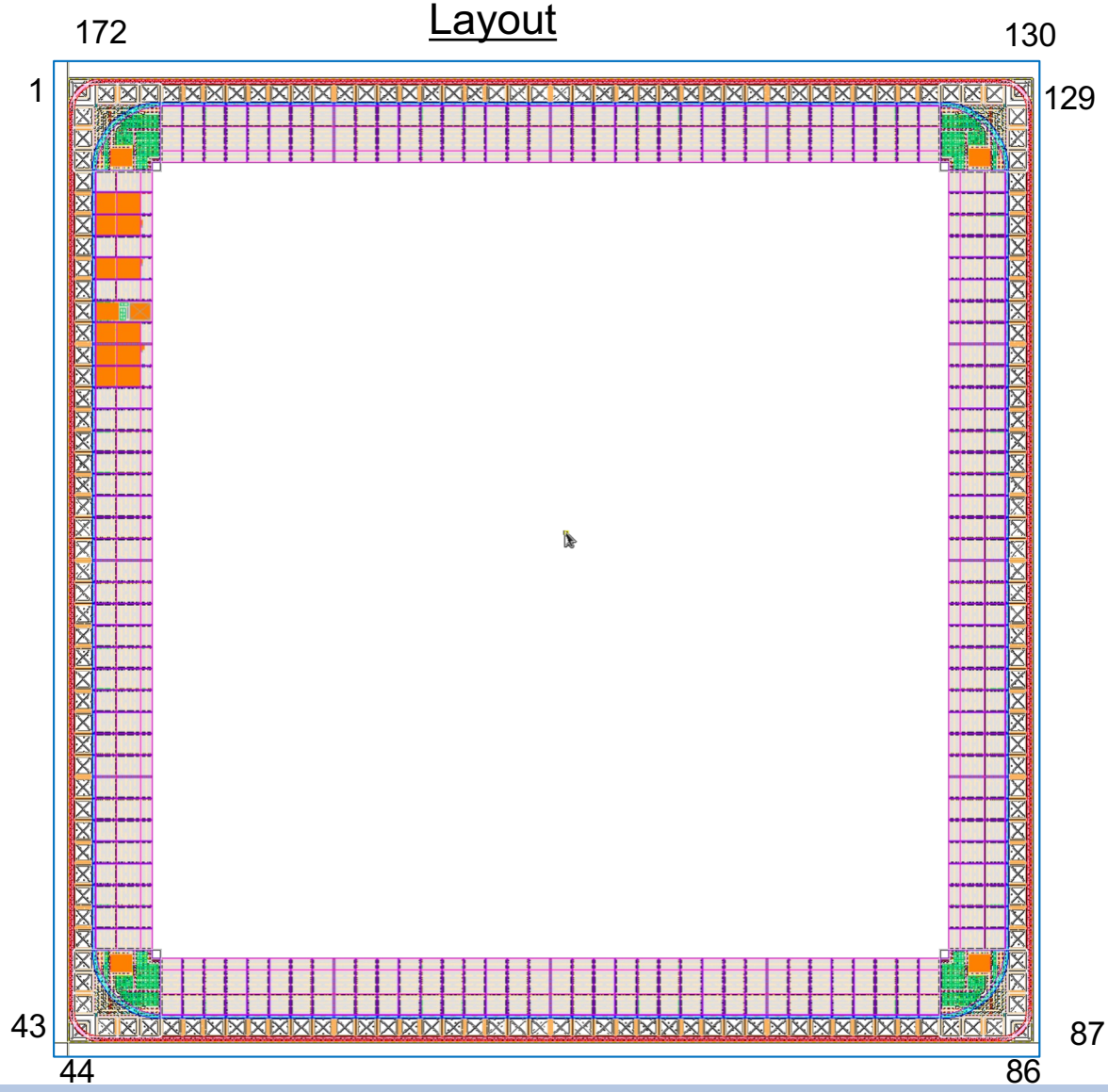
6. I/O Buffer rings

6-5. ioring45_5M5_1P8 (IO ring for 4.5mm chip (PGA178))

Schematic



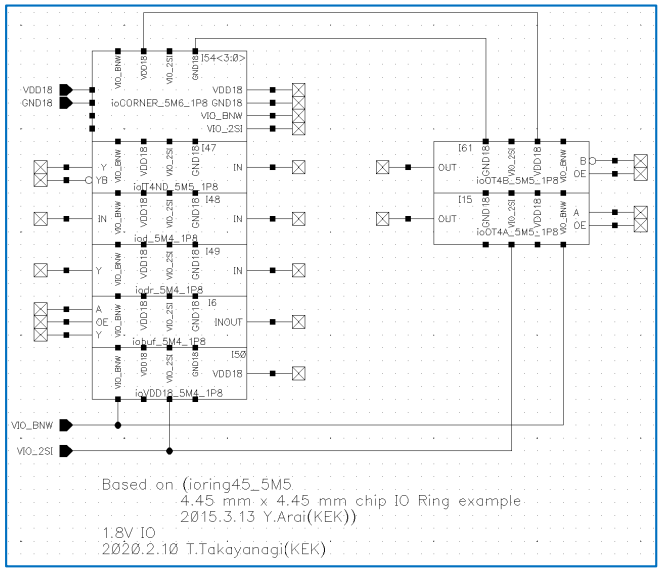
Layout



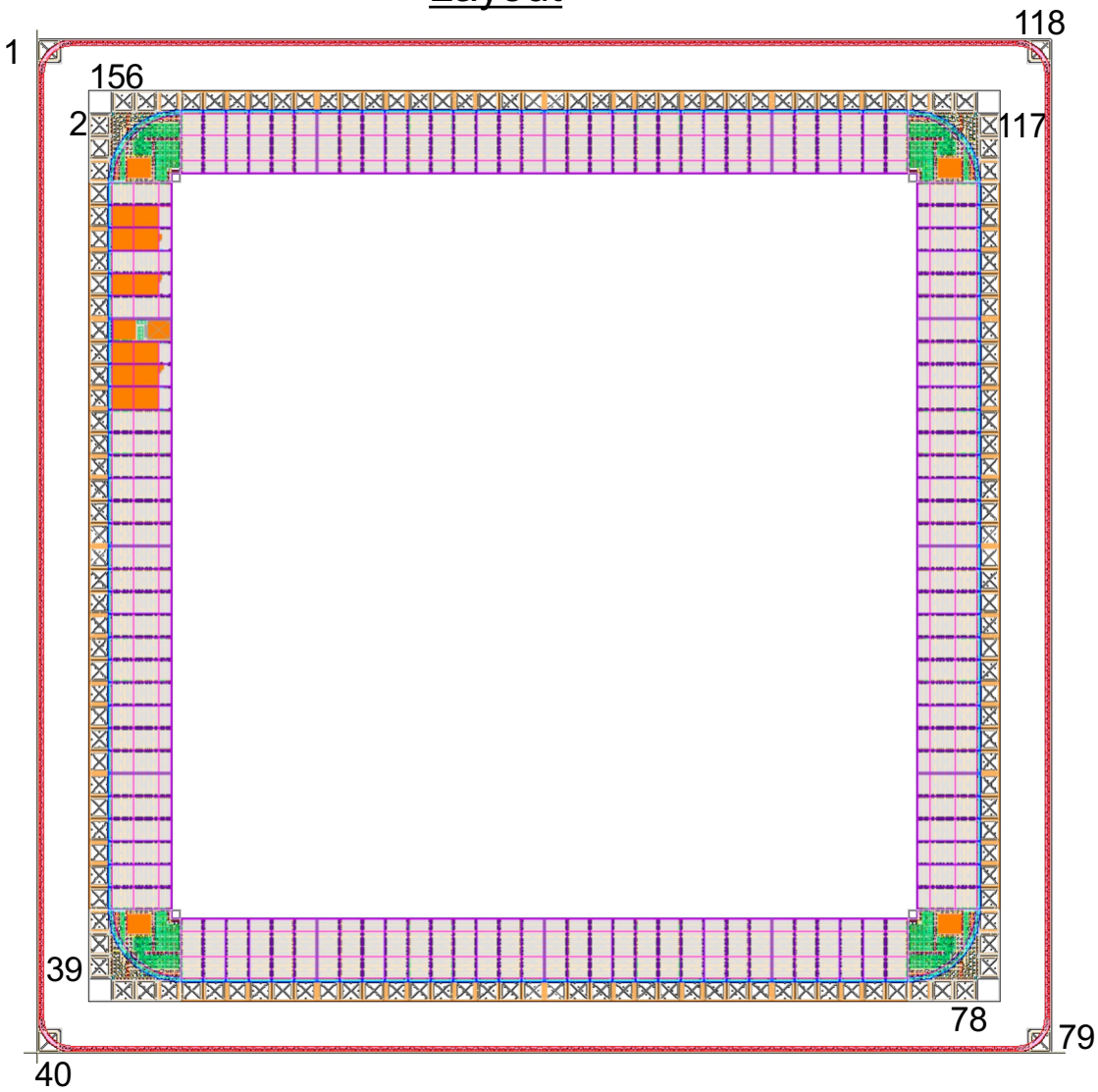
6. I/O Buffer rings

6-6. ioring45L2_5M5_1P8 (IO ring for 4.5mm chip with 200um bias spacing for pixel (PGA178))

Schematic



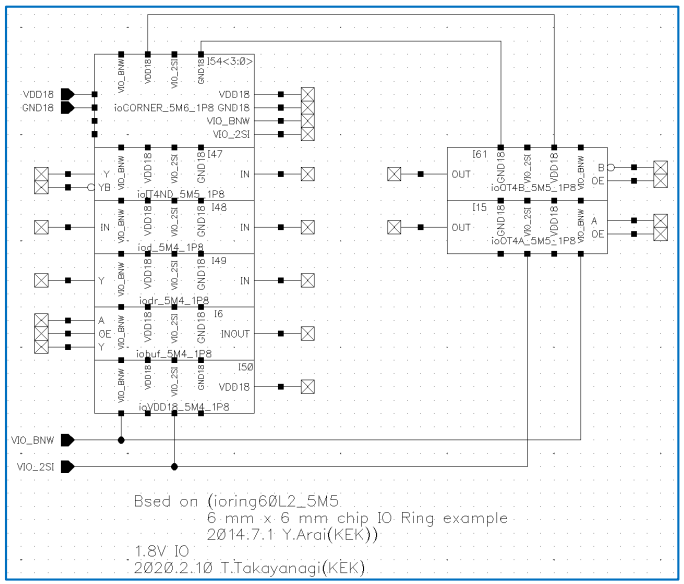
Layout



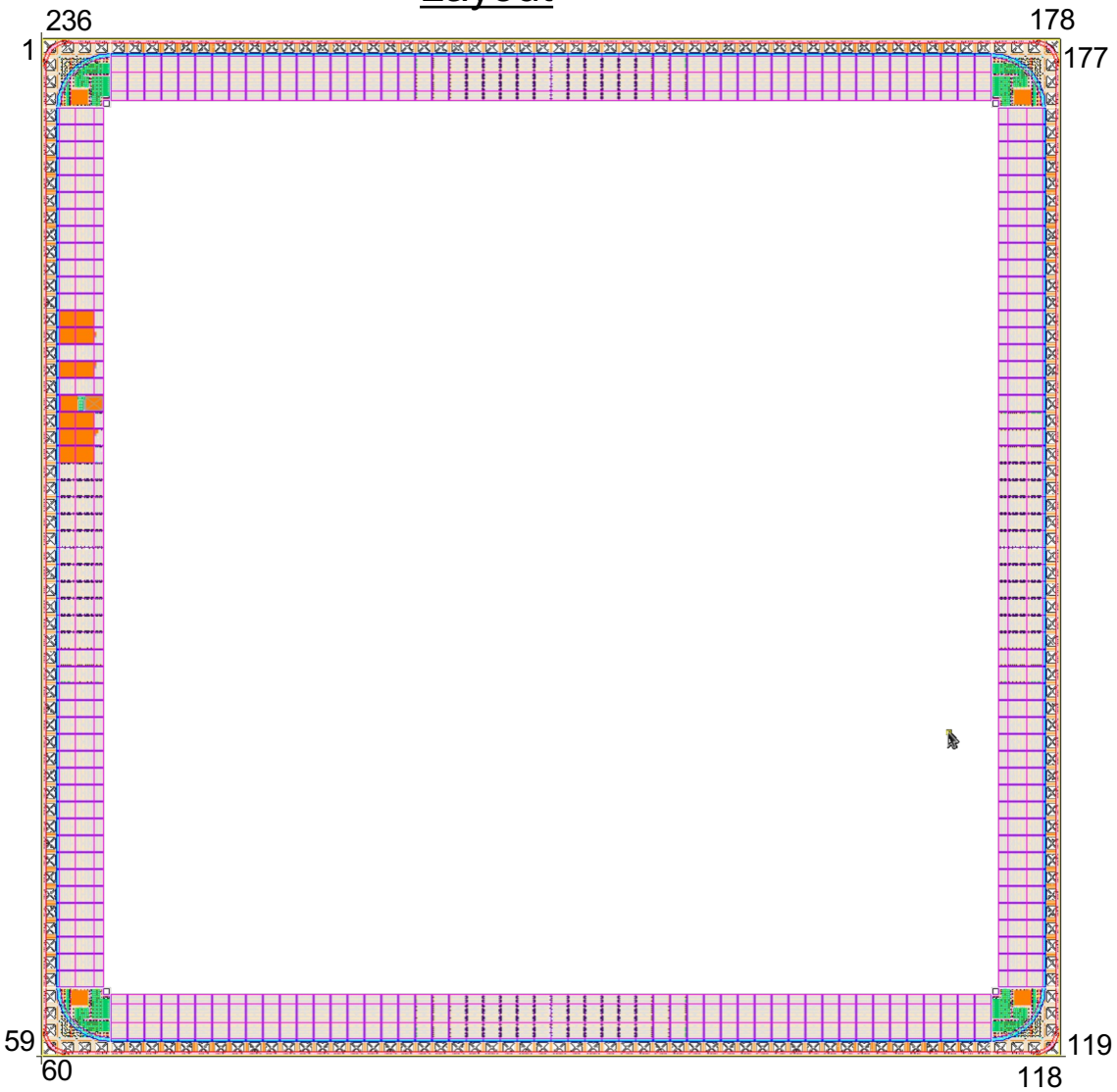
6. I/O Buffer rings

6-7. ioring60_5M5_1P8 (IO ring for 6.0 mm chip (PGA240))

Schematic



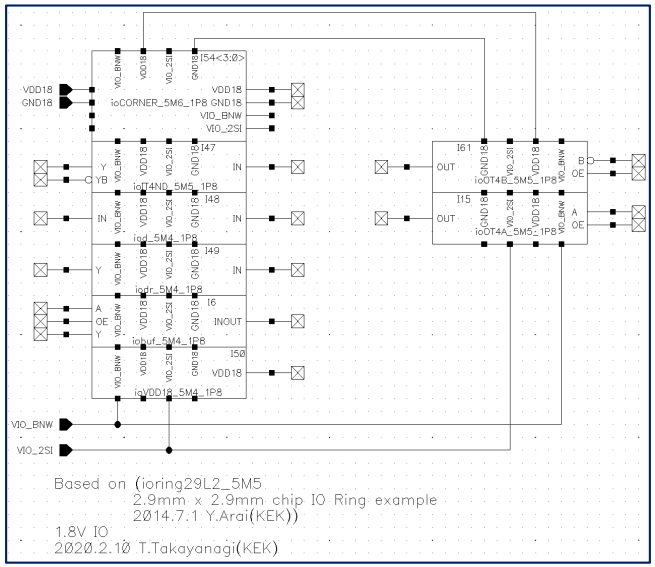
Layout



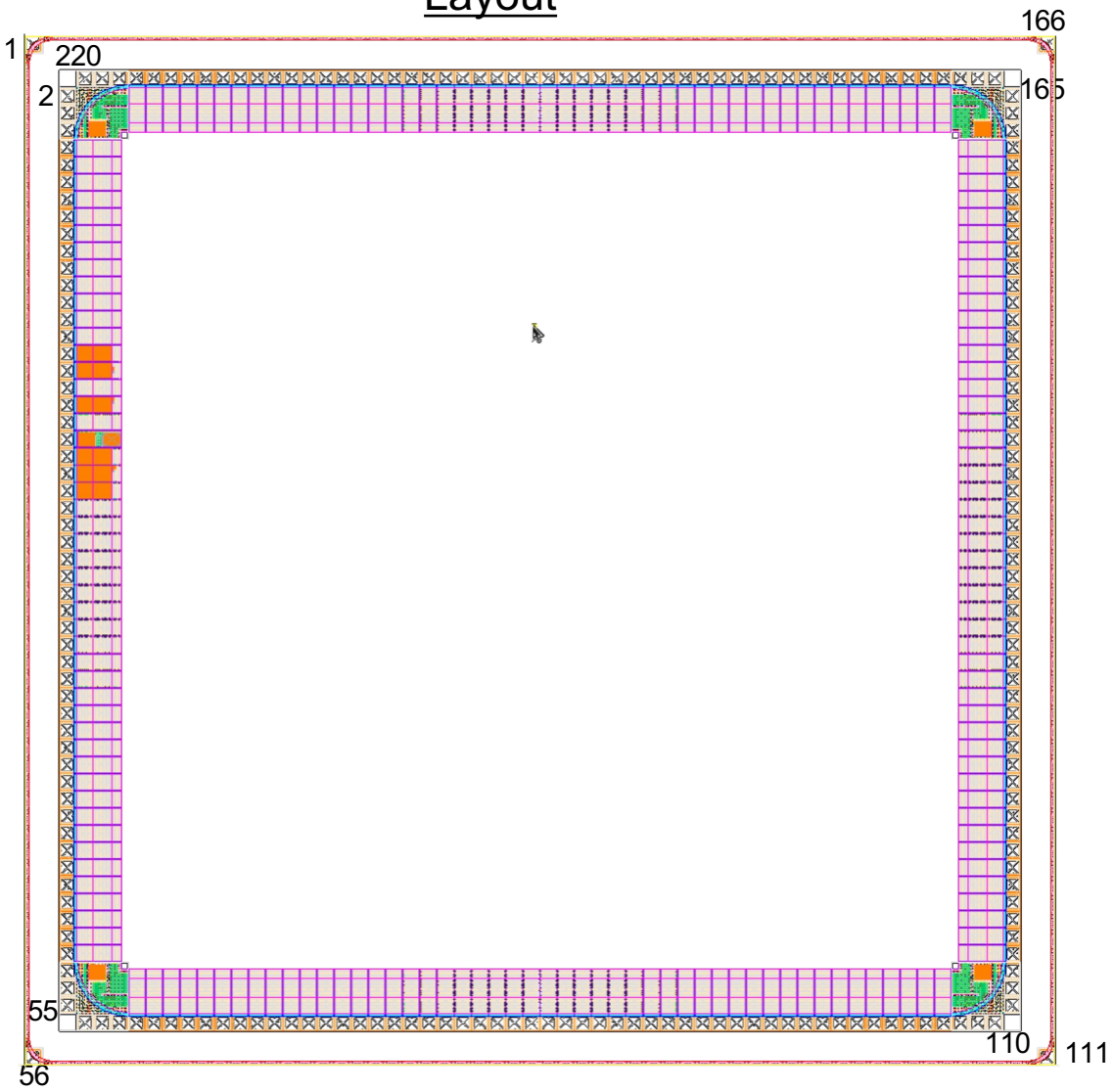
6. I/O Buffer rings

6-8. ioring60L2_5M5_1P8 (IO ring for 6.0 mm chip with 200um bias spacing for pixel (PGA240))

Schematic



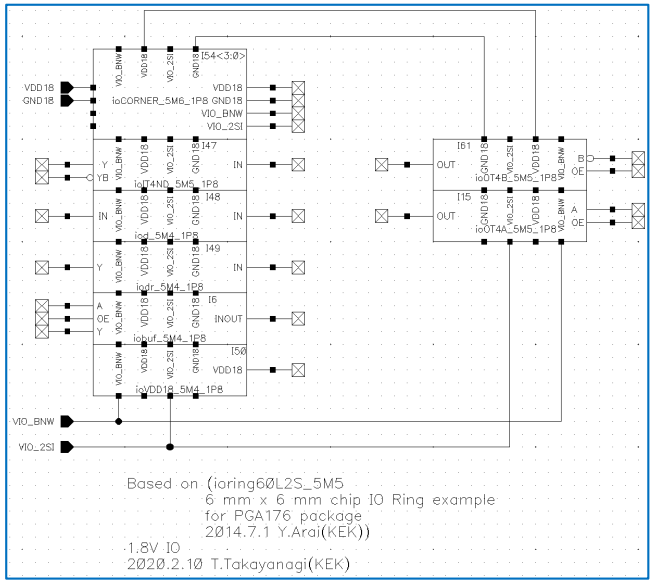
Layout



6. I/O Buffer rings

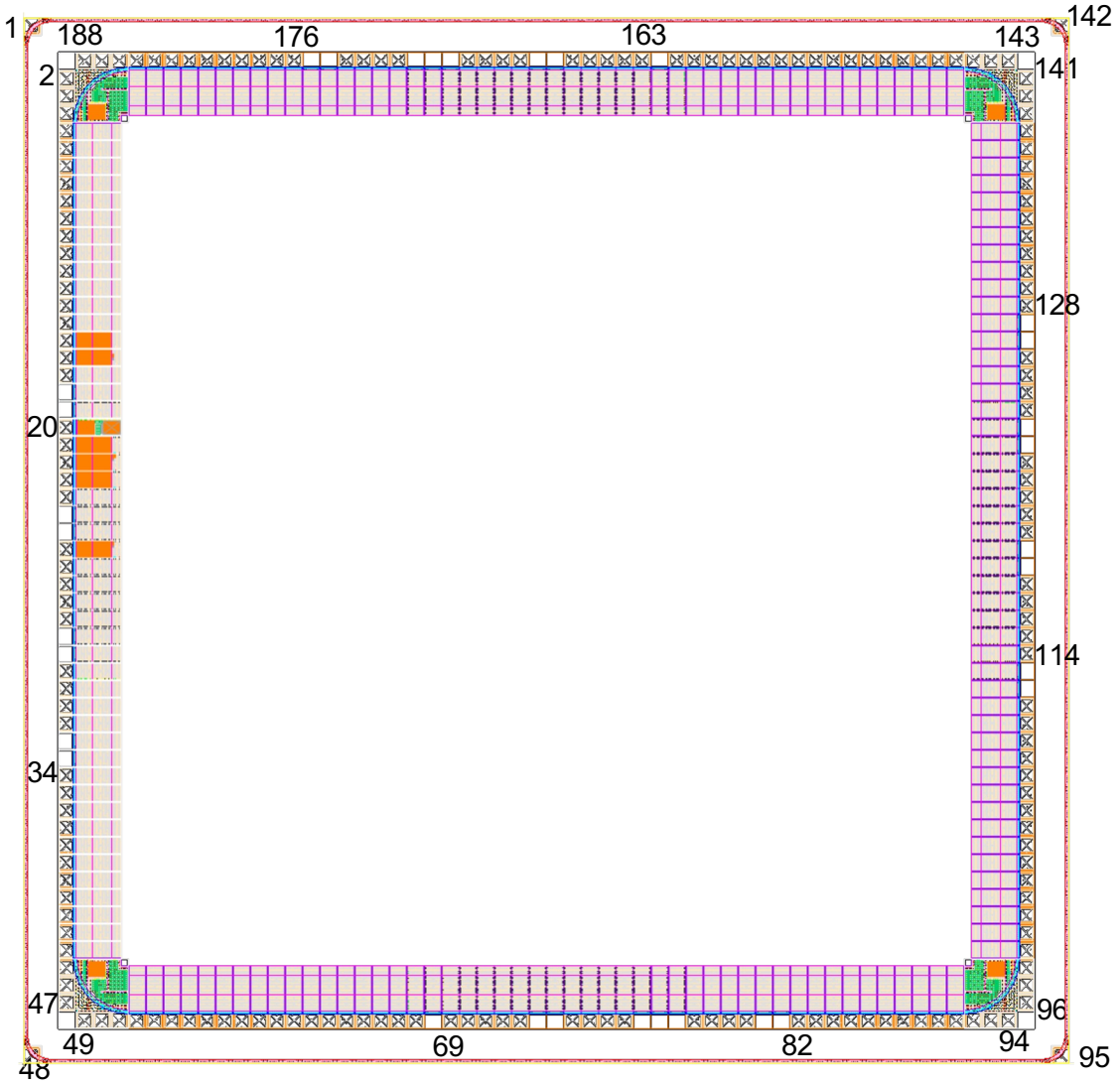
6-9. ioring60L2S_5M5_1P8 (IO ring for 6.0 mm chip with 200um bias spacing for pixel (PGA178))

Schematic



This chip can be packaged in PGA178 with no-connection of duplicated power/ground/bnw/soi2 connections.

Layout

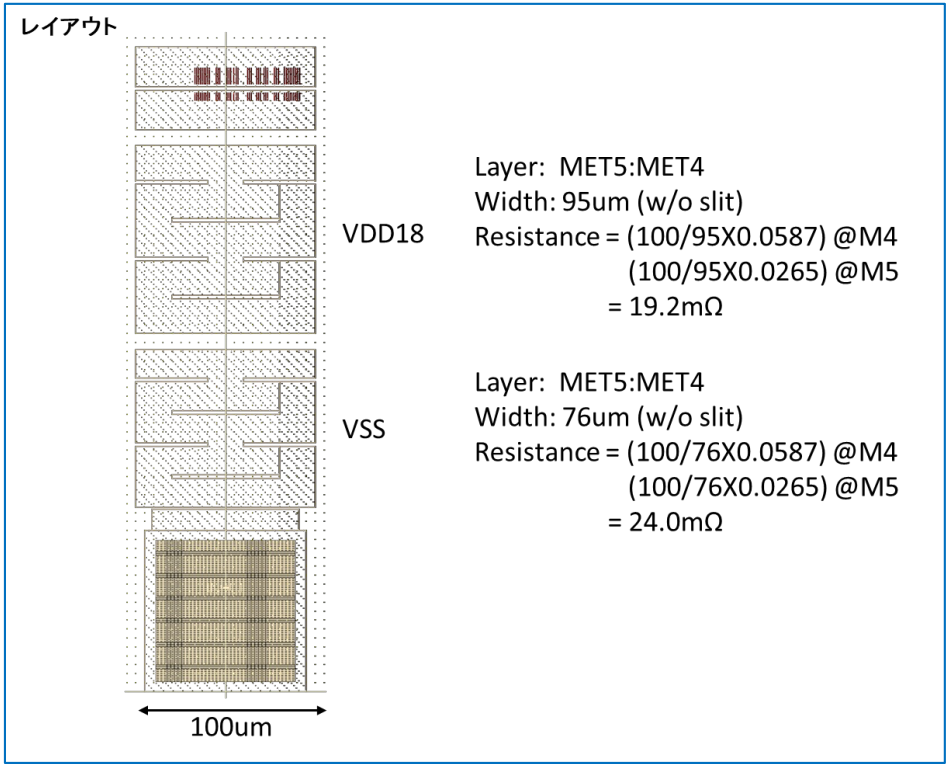


7. Appendix

Used Test Bench List

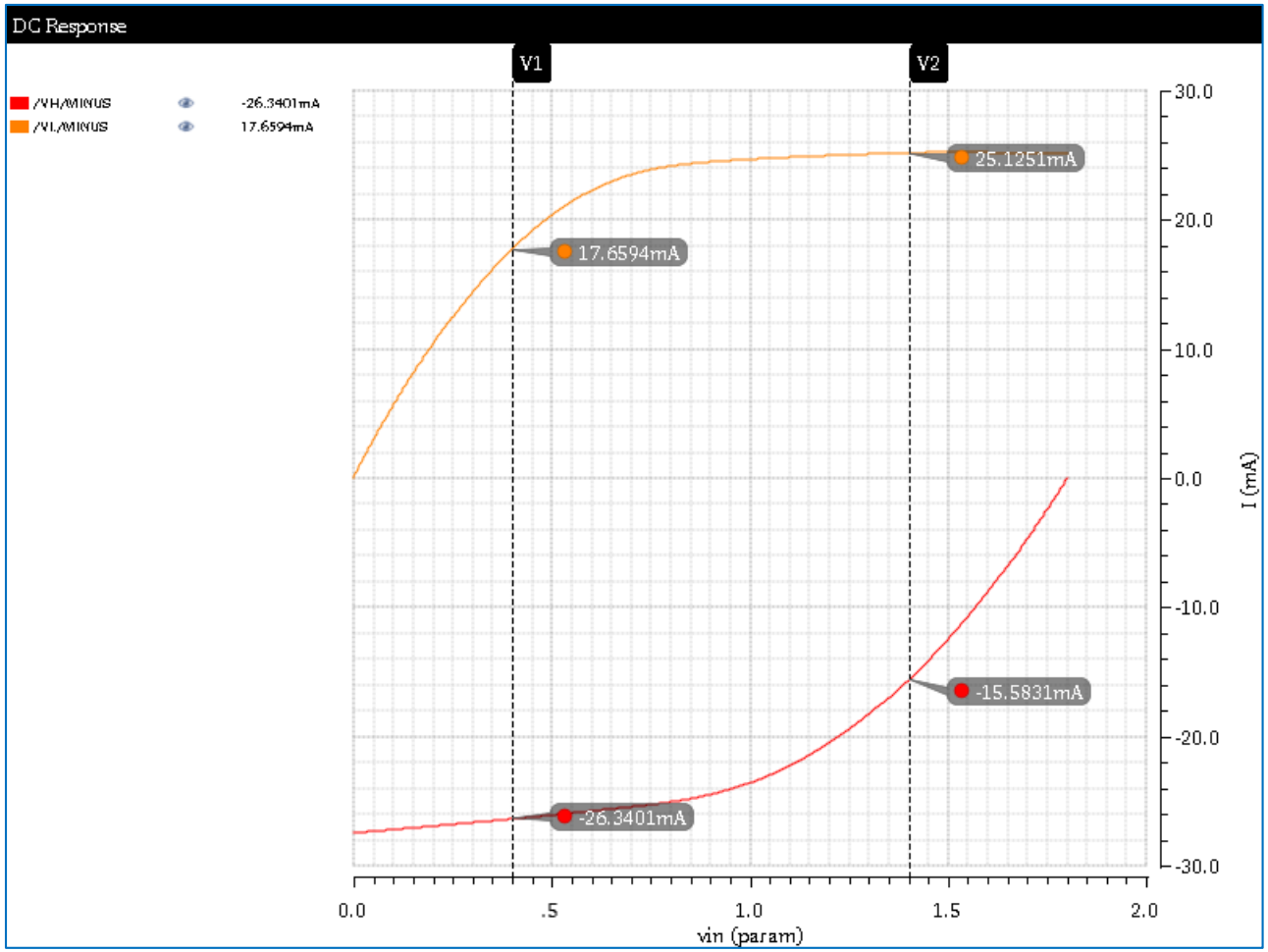
Degital buf	TB_iobuf_5M4_1P8_DC
	TB_iobuf_5M4_1P8_TRAN
	TB_iobuf_5M4_1P8_TRAN_post
	TB_iobuf2_5M4_1P8_TRAN_post
	TB_ioIT4ND_5M5_1P8_DC
	TB_ioIT4ND_5M5_1P8_TRAN_post
	TB_ioIT4NDP_5M5_1P8_DC
	TB_ioIT4NDP_5M5_1P8_TRAN_post
	TB_ioIT4N_5M4_1P8_TRAN_post
	TB_ioOT4A_5M5_1P8_TRAN_post
	TB_ioOT4B_5M5_1P8_TRAN_post
Analog buf	TB_AOBUF_1P8_RR_DC
	TB_AOBUF_1P9_RR_DC_post
	TB_AOBUF_1P8_RR_AC
	TB_AOBUF_1P8_RR_AC_post
	TB_AOBUF_1P8_RR_VF_AC
	TB_AOBUF_1P8_RR_VF_AC_post
	TB_AOBUF_1P8_RR_TRAN
	TB_AOBUF_1P8_RR_TRAN_post

Power GND resistance



7. Appendix continued

Digital Output Buffer IOH/IOL



<Condition> Tr:Typical, VDD18=1.8V, Tj=25deg, VOL=0.4V,VOH=1.4V

IOH	IOL	unit	target	Judge
-15.5	17.6	mA	|4mA|>	OK