

DIPIX1/2 User's Manual

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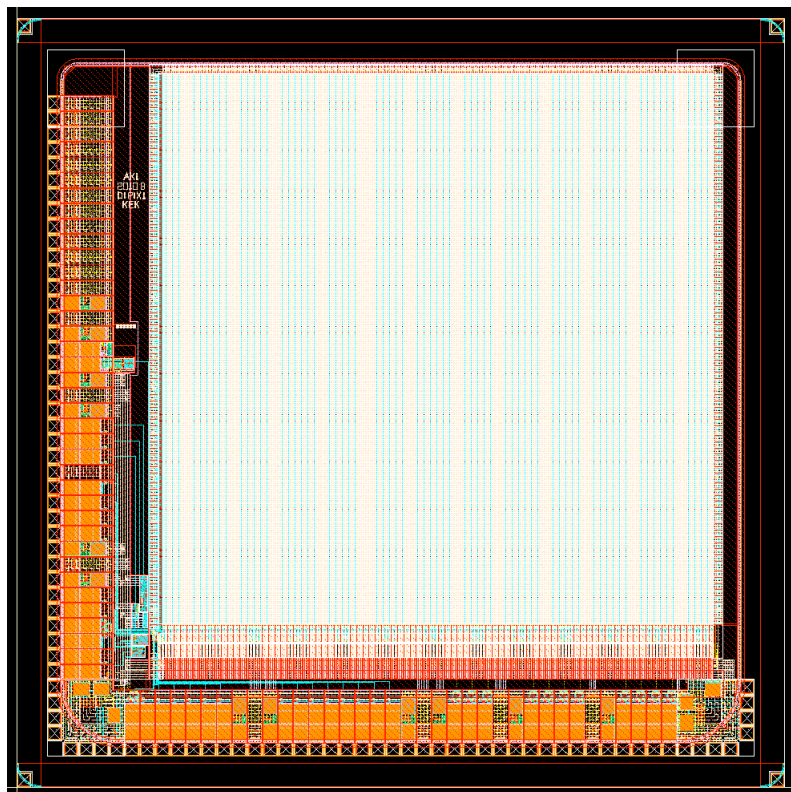
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Errata

1. Introduction

DIPIX1 and DIPIX2 chips are processed in the OKI Semiconductor CMOS FD-SOI 0.2 μ m pixel process developed at KEK. These chips include 14 μ m x 14 μ m size integration type pixels with CDS (Correlated Double Sampling) circuit. DIPIX1(256 x 256 pixel) and DIPIX2(256 x 128 x 2 type) have same circuit but have different sensor geometry in buried layers.

The circuit is designed to work both in n-type and p-type substrate. In addition, you can readout from analog output and/or digital output. Thus we named these chips as DIPIX (Dual mode Integration type PIXel) .

Layout size of the chip is 5.0 mm square, and actual dimension after dicing is about 5.1 mm square. The chip is typically thinned to 260 μ m (+10 μ m -20 μ m) by mechanical gliding and chemical etching, and 200nm Al sputtering is done in some case. There are bare chips and packaged chips in 177 pins ceramic package.

2. Circuit

2.1. Architecture

ピクセル回路を Fig. 1、チップの全体ブロックを Fig. 2 に、チップレイアウトを Fig. 3 に示す。

従来の INTPIX と同様のアナログ読み出しの他、各列に 10 ビットの Wilinson 型 ADC があり、これを使ったデジタル読み出しも行える。また、Address Decode によるデッドエリアを減らすため、Row/Column Address Decoder の代わりにシフトレジスターに置き換えている。このため、ランダムアクセスは出来ず端から順次アドレス指定をしていく必要がある。

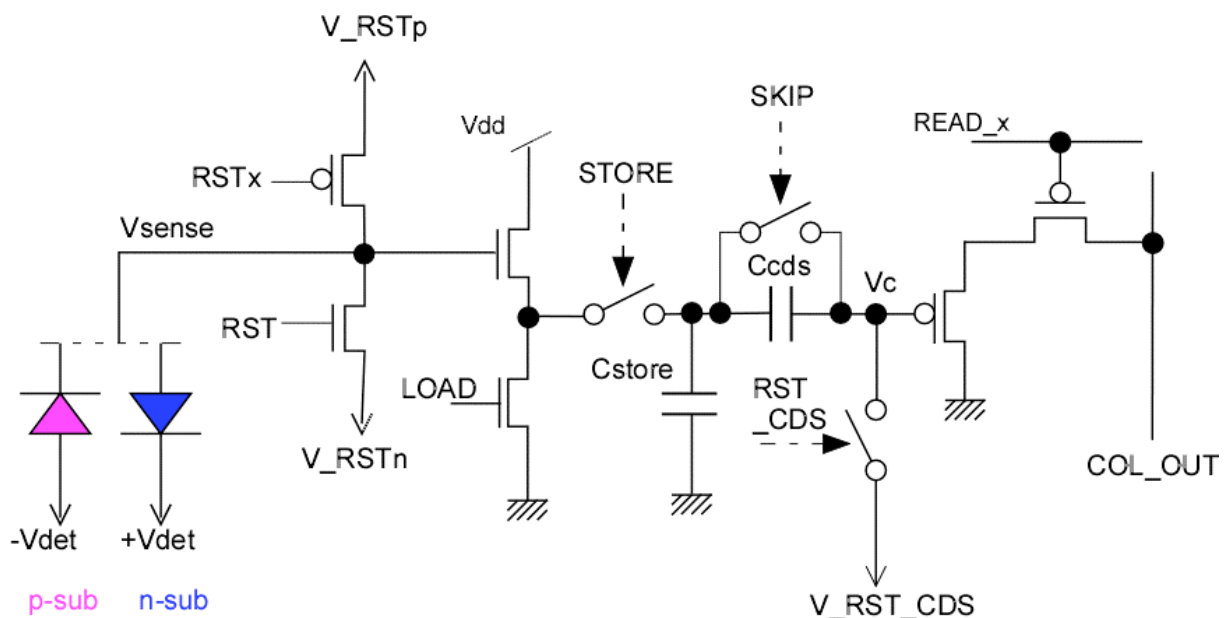


Fig. 1 Schematics of DIPIX1/2 pixel.

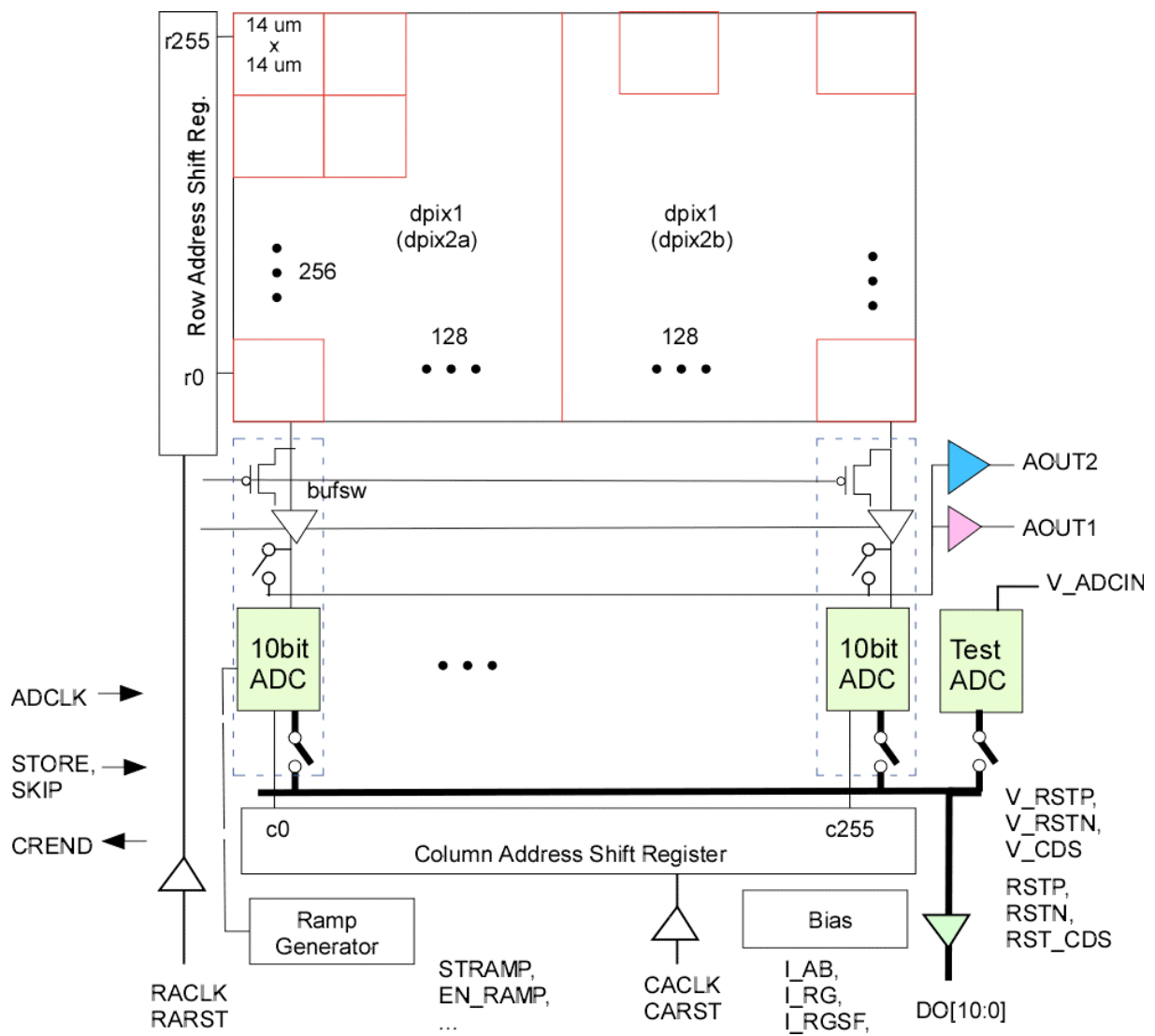


Fig. 2. Block diagram of DIPIX1/2. DIPIX1 has one 256×256 pixel array, and DIPIX2 has two kinds of 256×128 pixel arrays.

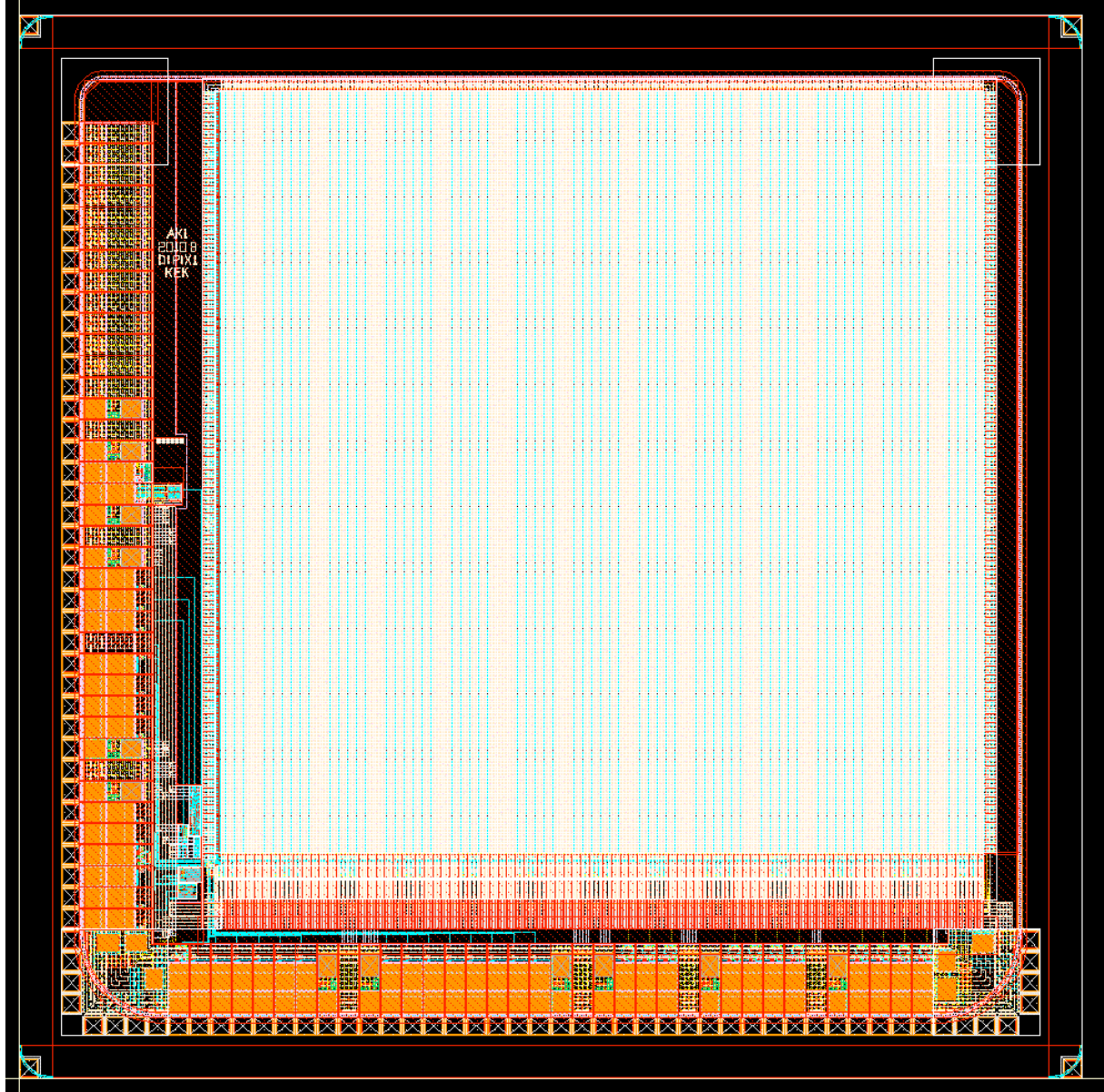


Fig. 3 Chip layout of DIPIX1/2.

2.2. Potential Rings

チップ外周には HV Ring (=VDET)が配置されていて、センサー部への電圧は VDET または底面 (=VBACK)より印可することが出来る。

アクティブな回路の再外周は PSUB ring(Bias Ring)により囲まれ、これは VBIAS 端子に繋がっている。またピクセルアレイの外側も PSUB ring により囲まれており、周辺回路の底面に配置された BPW/PSUB/Metal1 と共にすべて VBIAS 端子に繋がれている。

2.3. Pixel

Fig. 1 にピクセル回路を示したが、これらは基板タイプに応じて Fig. 4 のようにバイアス電圧を変えることにより p 型基板及び n 型基板の双方に対応できる。詳細回路を Fig. 5 に、レベルダイアグラムを Fig. 6 に示す。

次にピクセルのレイアウトを Fig. 7 に示す。DIPIX1 には dpix1 セルが使用されている。DIPIX2 には dpix2a(column address 0~127)と dpix2b(column address 128~256) の 2 種類のピクセルが入っている。Pixel の大きさは 14 μ m x 14 μ m でレーザー光を照射できるように、中央部におよそ 5.5 μ m 角の Metal のない領域がある。このため蓄積用コンデンサーはずらして下のピクセルに半分かかる部分に置いてある。PSUB 電極は外形 1.4 μ m の十二角形の物を使い、その周りに幅 10 μ m の変形 8 角形の BPW が置い

である。詳細を Fig. 8～ Fig. 10 に示す。

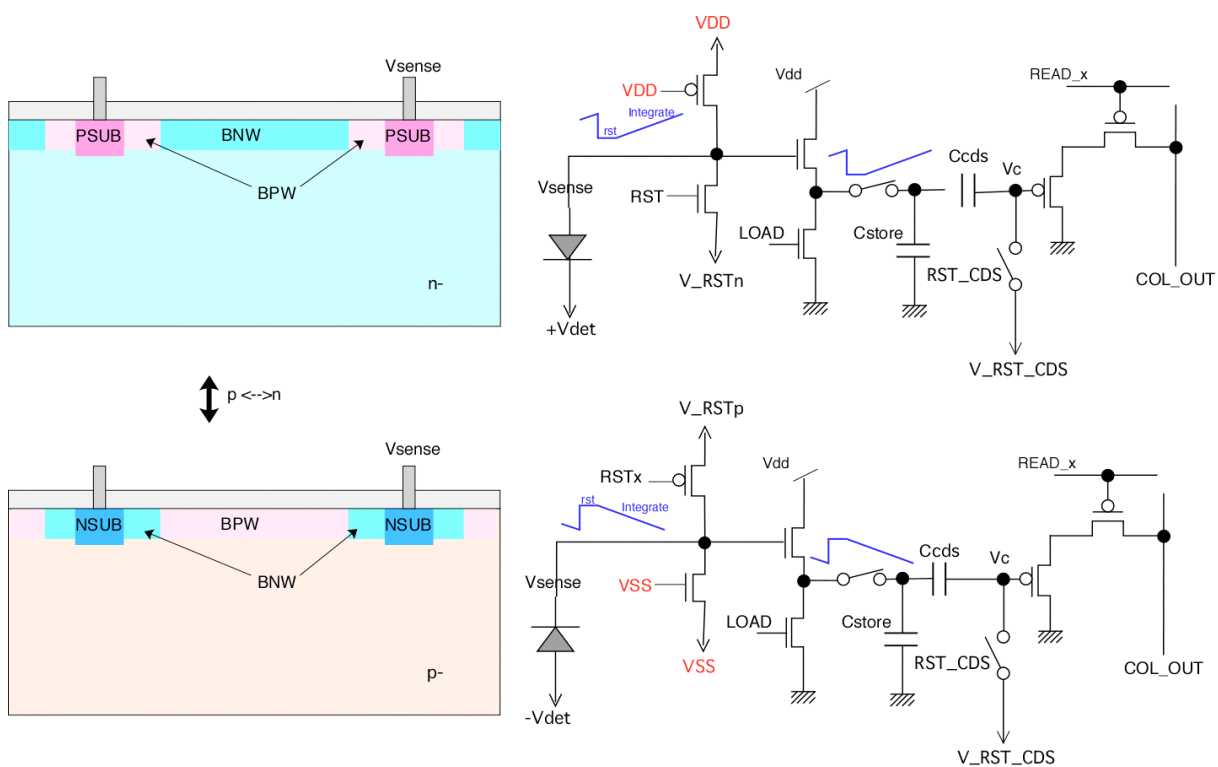


Fig. 4 Operations in p-sub and n-sub wafer.

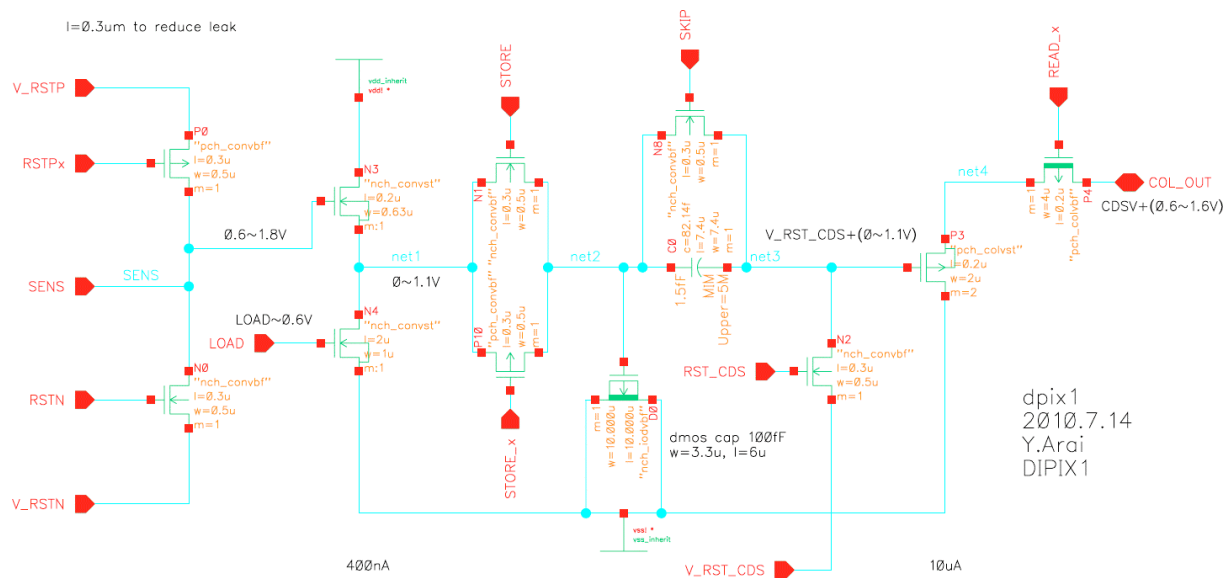


Fig. 5 Detailed pixel schematic

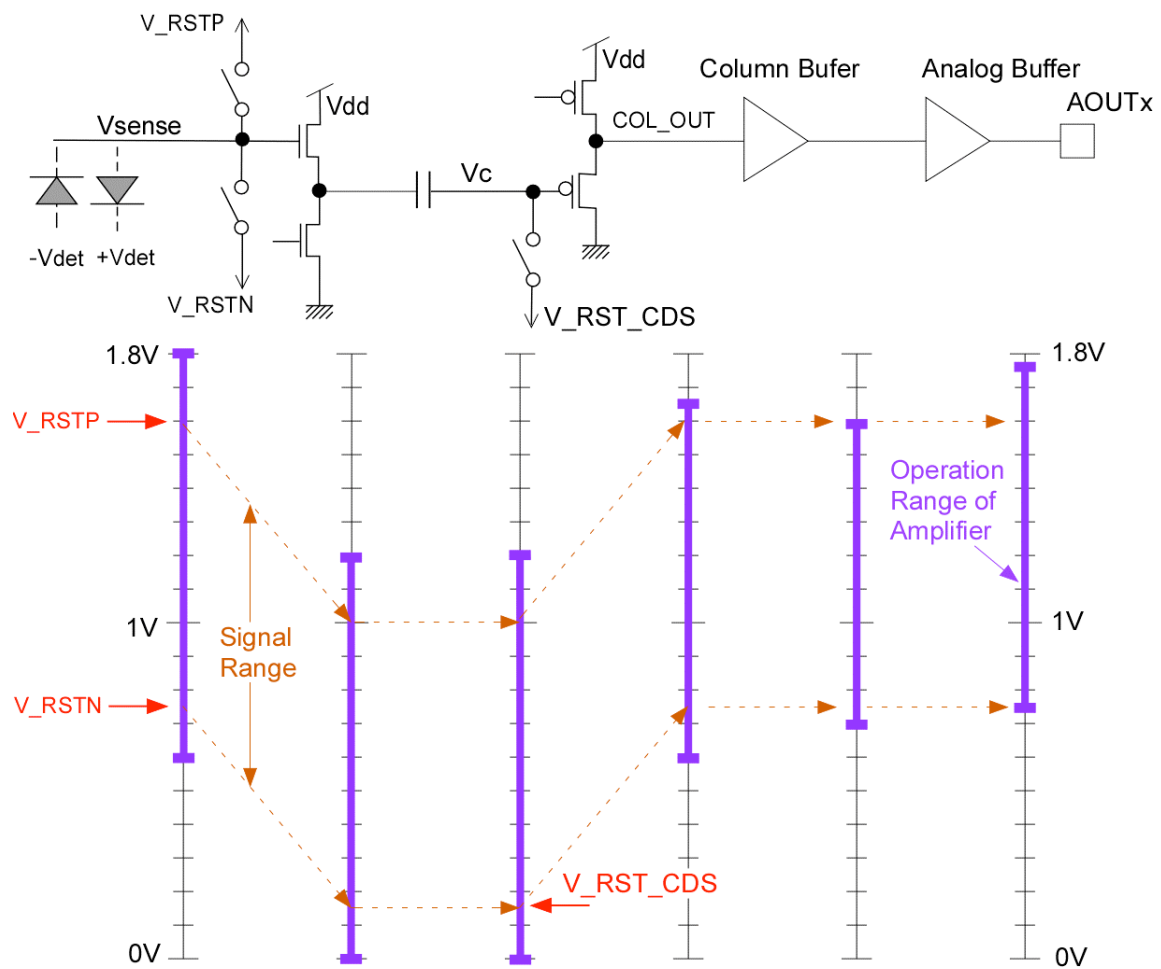


Fig. 6 Diagram of internal voltages.

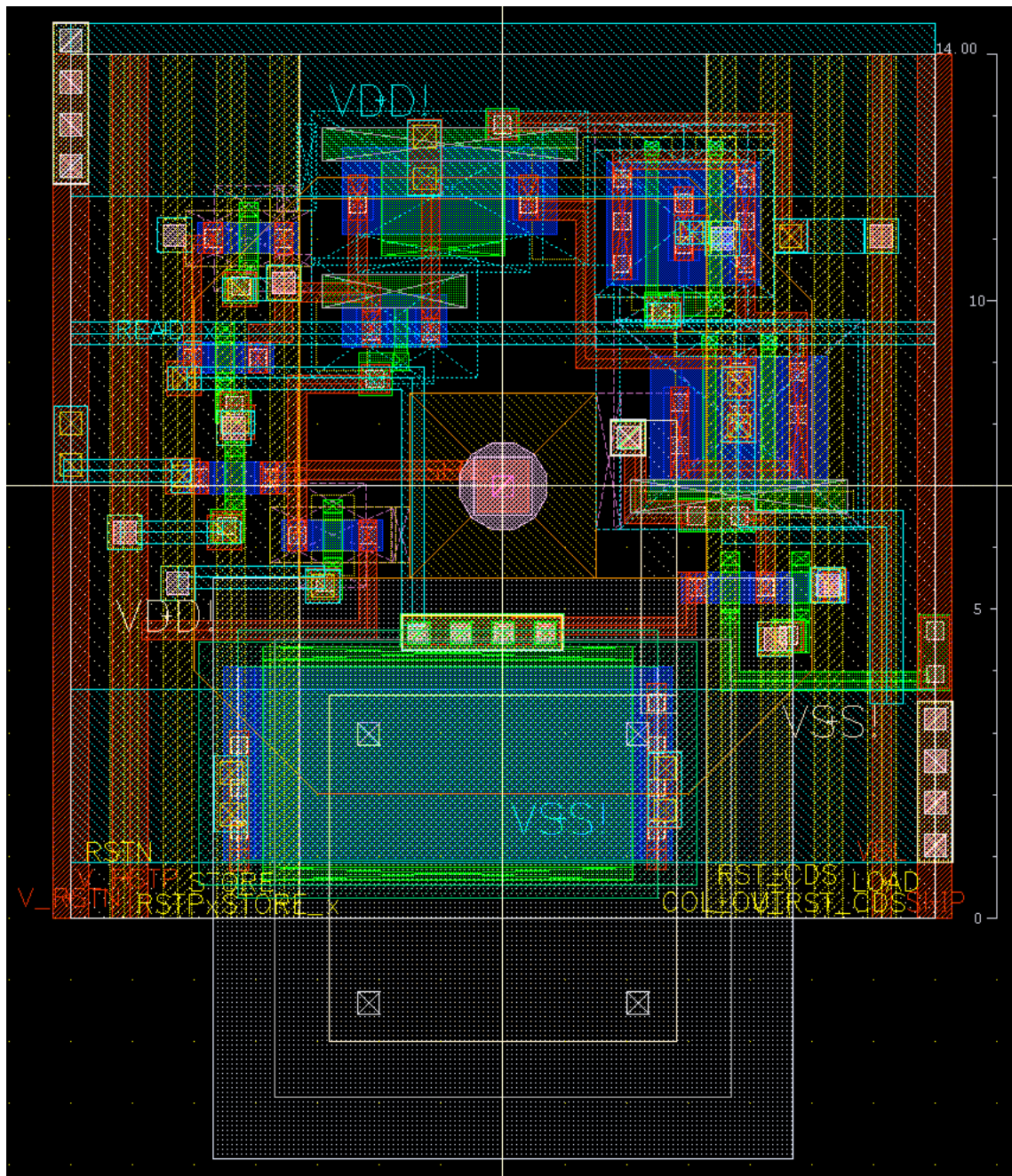


Fig. 7 Pixel layout of the dpix1. Pixel size is 14 μ m x 14 μ m . Lower white square is a capacitor. Center red octagon is BPW. Pixel in dpix2a, dpix2b has same layout in transistors and metal wire, but has different buried layer layout.

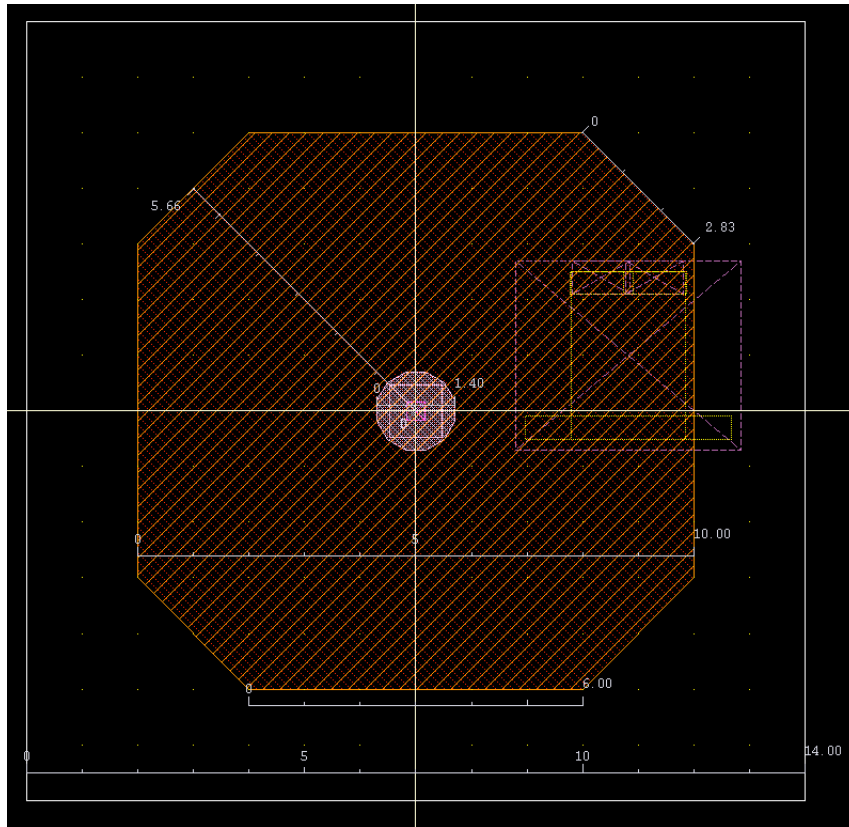


Fig. 8 Buried layer layout of dpix1. Both BPW and BP2 (deeper p well) has same layout.

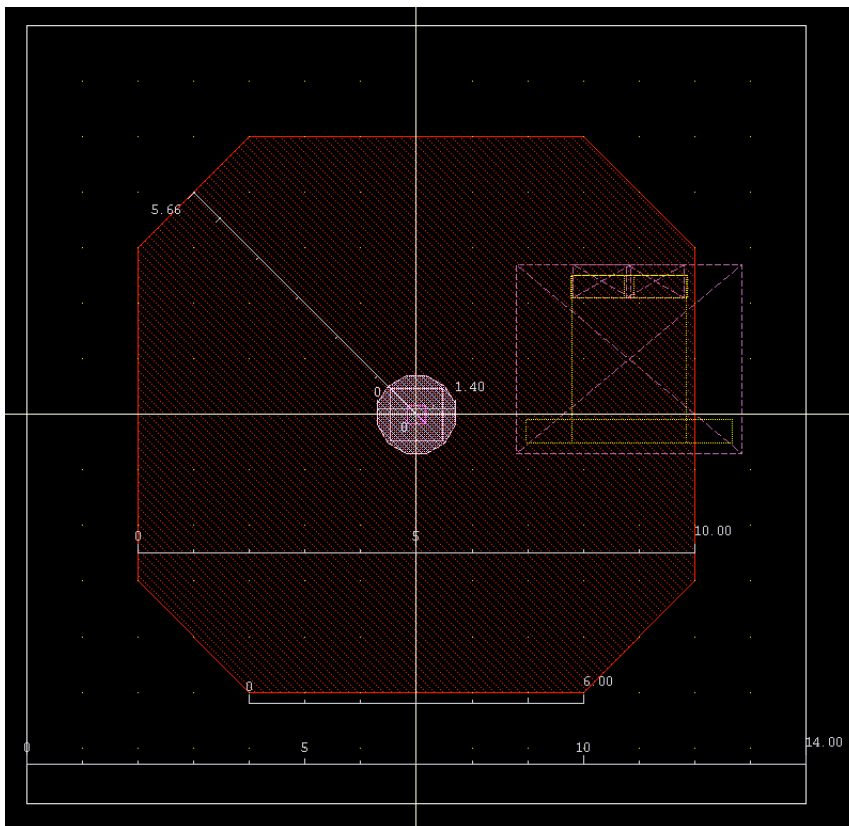


Fig. 9 Buried layer layout of dpix2a. There is no BP2 layer.

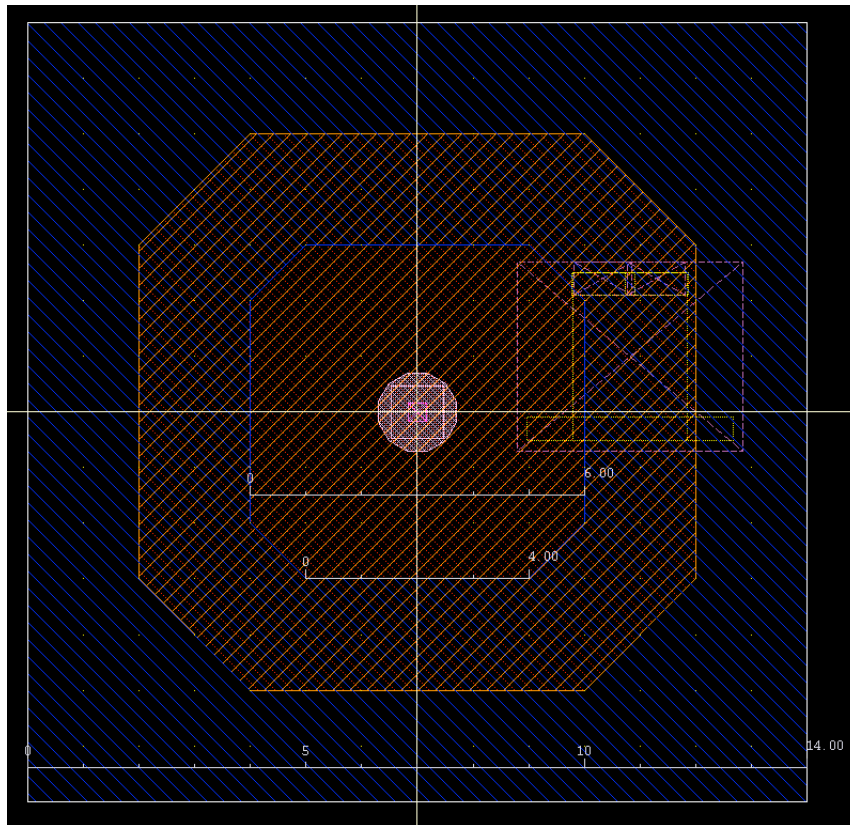


Fig. 10 Buried layer layout of dpix2b. In addition to the BPW and BP2, BNW layer (blue) is overwrapped. This pixel is designed for p-sub wafer and reverse implant, so the BNW layer act as p-stop(p spray) layer.

2.4. Shift Register for addressing

Row Address 及び Column Address は Shift Register により選択される。シフトレジスタをリセットすると全出力が 1（非選択状態）となり、その後、CLK 信号を 1 回送ると 1 行（列）目が 0（選択状態）となり、CLK パルス毎にひとつずつ移動して行く。ループはしていないので、最後のチャンネルまでシフトした後は必ずリセットが必要。シフトの向きは、図 2 で Row 側が上方向、Column 側が右方向へ進む。

2.5. Column ADC

Column ADC の動作概要を Fig. 11 に示す。

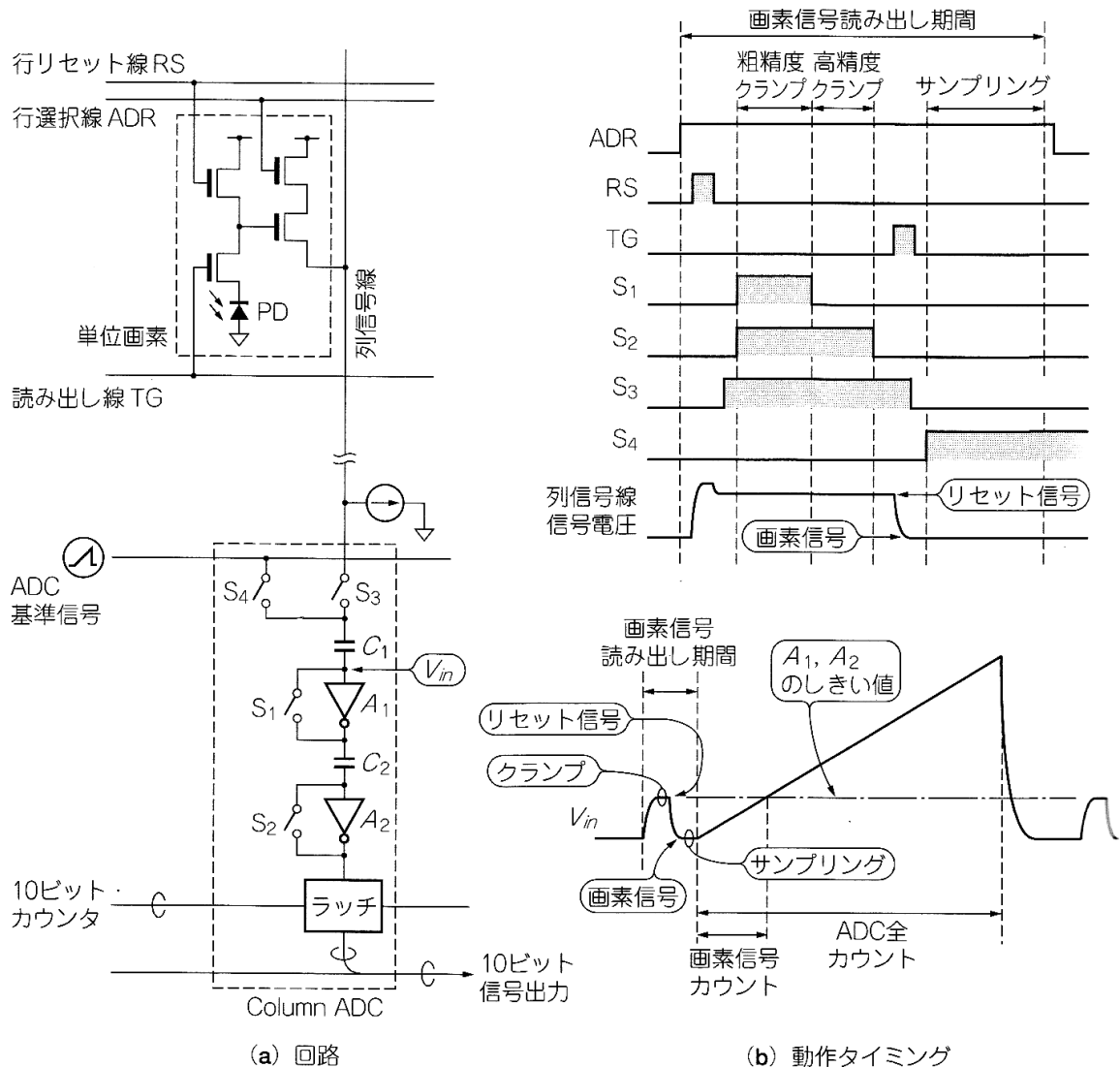


Fig. 11 Principle of Column ADC.

2.6. Signal Delay & Delay Monitor

DIPIX では CDS 回路と ADC 回路に於いて数 ns 離れた連続した信号が必要とされる。これらの信号を FPGA で生成して送り込んでも良いが、FPGA で生成する場合は、最低 1 クロック分(~数十 ns)離れる事になってしまう為、読み出し時間が長くなってしまう。

また将来的には、これらの信号をチップ内部で生成し、外部信号の数を減らすようにしたいため、今回以下のような遅延回路を内部に設けた。

遅延+モニター回路の構成を Fig. 12 に示す。外部からの RST_CMP1 信号は入力バッファを通った後、内部回路に直接供給されるが、RST_CMP2 信号は vcdelay 回路を通して遅延された後に内部回路に供給される。つまり vcdelay の遅延を正しくセットすれば、RST_CMP1 と RST_CMP2 とは同じタイミング信号を入力すれば良いように出来る。

但しこのままだとどれくらい遅延させたのか判らないので、MDEL 端子に遅延時間に相当する時間幅のパルスが出るようにした(Fig. 14)。

RSTN(又は RSTP)端子と RSTCDS 端子に関しても同様の設定が行える。

vcdelay の回路図を Fig. 13 に示す。N7 及び N1 のトランジスタに流れる電流を制限する事により遅延を制御している。V_DCON を 0 V にすると信号は通らなくなるので、遅延回路を使わない時は V_DCON を 1.8V にしておくが良い。

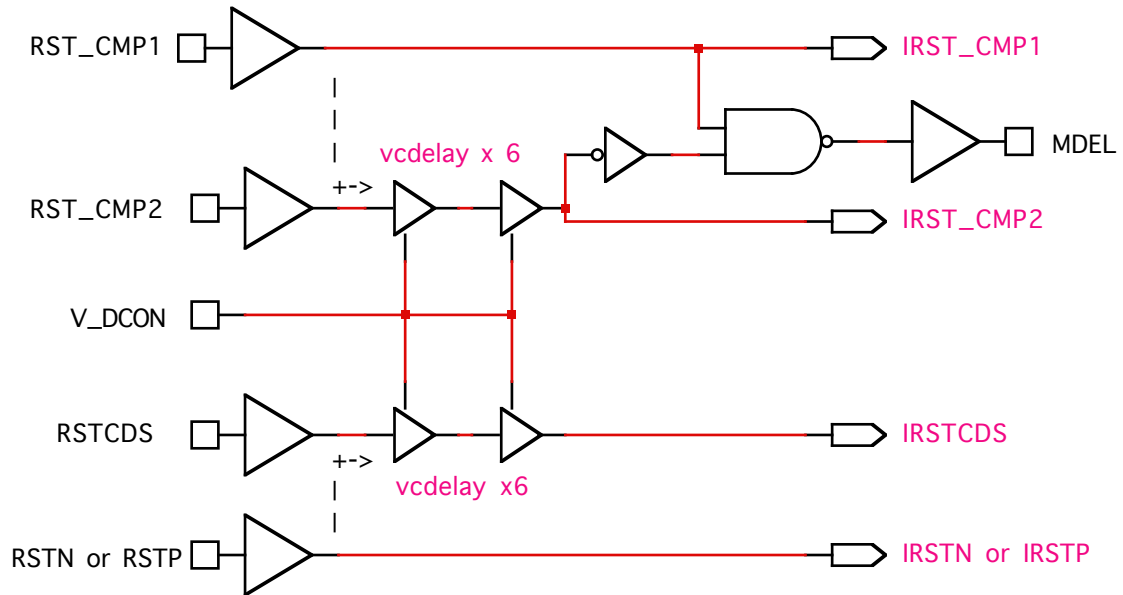


Fig. 12 Signal Delay and Delay Monitor circuit.

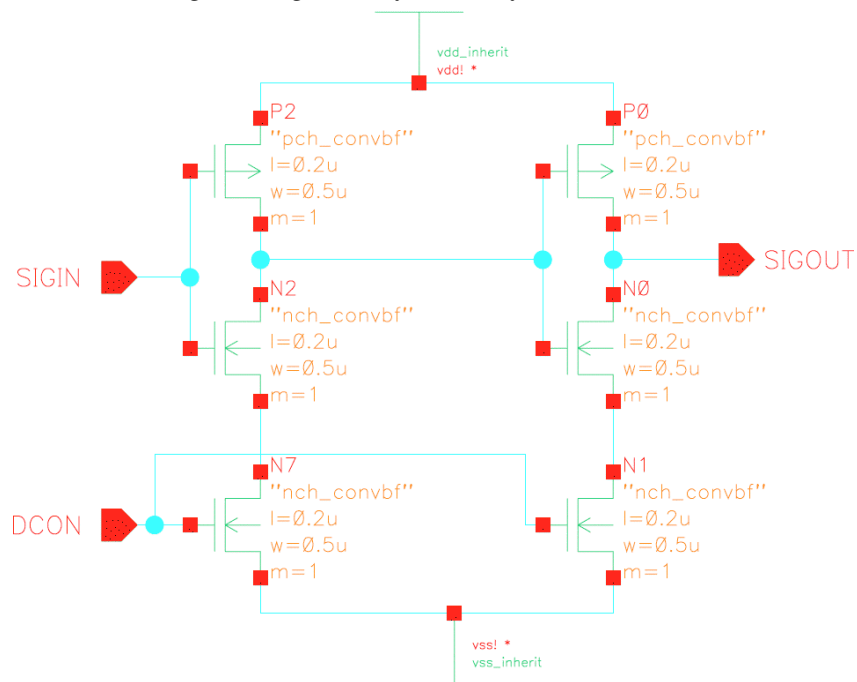


Fig. 13 Variable delay circuit.

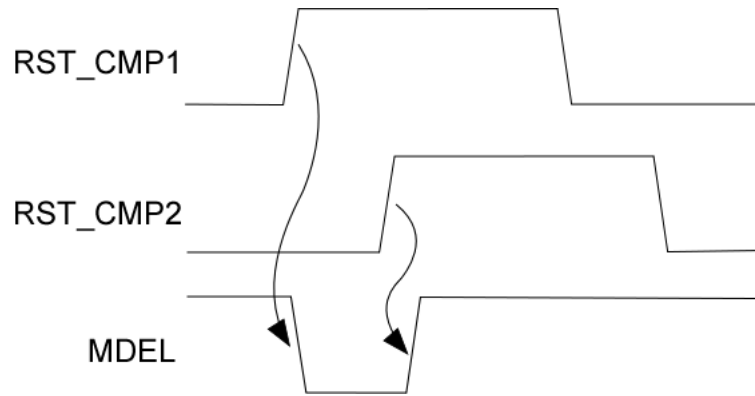


Fig. 14 Timing of the Signal Delay & Delay Monitor circuit. The rising edge timing difference between RST_CMP1 and RST_CMP2 will be the pulse width of MDEL.

3. Signal & Timing

各種信号の説明とタイミングを以下に示す。

3.1. Digital Signals

All the digital signal has 3.3V CMOS level (threshold $\sim 1.65V$).

- DO[10:0]
ADC Output Data
- CARSTx
Reset signal for Column Address shift register. When this signal is issued CA become -1 (none of the column is selected) and the Test ADC is selected.
- CACLK
Clock signal for Column Address shift register. In each clock, next column (+1) is selected. The shift register does not circulate and the end of column can be confirmed by looking 'CRENDx' signal.
- RARSTx
Reset signal for Row Address shift register. When this signal is issued (low level), RA become -1 (none of the row is selected)
- RACLK
Clock signal for Row Address shift register. In each clock, next row (+1) is selected. The shift register does not circulate and the end of row can be confirmed by looking 'CRENDx' signal..
- RSTN
Reset control signal for n-type substrate. In p-type substrate, connect to VSS. When RSTN=Hi Vsense node is connected to V_RSTN voltage.
- RSTP
Reset control signal for p-type substrate. In p-type substrate, connect to VDD. When RSTN=Hi Vsense node is connected to V_RSTP voltage.
- RSTCDS

Reset control signal for CDS circuit. By asserting this signal one terminal of the Cds capacitor is connected to V_RST_CDS voltage. You can connect same signal as RSTP/N when you use internal delay circuit which is controlled with V_DCON signal. (see 2.6)

- RST_CMP1

Reset signal for the first stage comparator in the Column ADC.

- RST_CMP2

Reset signal for the first stage comparator in the Column ADC. You can connect same signal as RST_CMP1 when you use internal delay circuit which is controlled with V_DCON signal.(see 2.6) . The delay can be checked with MDEL signal.

- MDEL

Monitor signal of delay between RST_CMP2 and RST_CMP1.

- STORE

STORE control signal in the pixel.

- SKIP

SKIP control signal in the pixel. When this signal is Hi, Cds capacitor is shorted.

- EN_RAMP

Enable Ramp signal to Comparator. By asserting this signal, Ramp signal is applied to comparator of the column ADC.

- EN_PIX

Enable Pixel signal to Comparator. By asserting this signal, Pixel output signal is applied to comparator of the column ADC.

- RST_CNTx

Reset signal for counters of Column ADCs.

- ADCLK

Clock signal for Column ADC. The counter is counted with this signal.

- STRAMPx

Start control signal for the Ramp Generator. By asserting this signal, ramp signal start to increase.

- CRENDx

Monitor output of end of Row Address shift register or end of Column Address shift register. When the last shift register (CA or RA=255) is selected, this signal becomes Lo.

3.2. Analog Signals

(Caution : The value shown below is derived from simulation when the sensor bias is 0V. The value may be changed in real situation.)

- I_PIX

Reference current for load voltage in pixel, Column Buffer, AOUT1 analog output buffer (AOBUF). Typical value is 20 uA (Connect ~60KOhm resistor to 1.8V).

- I_AB

Reference current for AOUT2 Analog Buffer (AROAobuf33_30_WIESD designed by A-R-Tec). Typical value is 36uA.

- I_RG

Reference current for Ramp Generator. Typical value is ~1uA.

- I_RGSF

reference current for Ramp Generator Source Follower circuit. Typical value is ~10uA.

- V_RSTN

Reset voltage for n-type substrate. Nominal value is ~0.2V. In case p-type substrate, connect this signal to VSS.

- V_RSTP

Reset voltage for p-type substrate. Nominal value is ~1.6V. In case n-type substrate, connect this signal to VDD18.

- V_RST_CDS

Reset voltage for CDS circuit. Nominal value is ~0.15V.

- VBL

Bias line of Pixel. Not used.

- V_ADCIN

Test input of the Test ADC circuit. The ADC is enabled when CARSTx becomes Lo.

- V_DCON

Control voltage of Delay circuit. When this signal is 1.8V, the delay will be minimum. If this signal is connected to VSS, the delay circuit does not work.

- V_RAMP

Ramp Generator offset voltage. When the Ramp circuit is stopped by 'STRAMPx' signal, the ramp voltage returns to this voltage. Please set to desired offset value or connect to ground through 1.1 kohm resistor (discharge time ~ 450 ns, see Fig. 15).

- AOUT1

Analog output signal #1. Output buffer of aobuf which has been used in previous chips is used. Output signal range is about 0.75~1.6V.

- AOUT2

Analog output signal #2. New output buffer of AROAobuf33_30_WIESD which is designed by A-R-Tec and occupy I/O buffer area is used. Output signal range is about 0.75~1.6V.

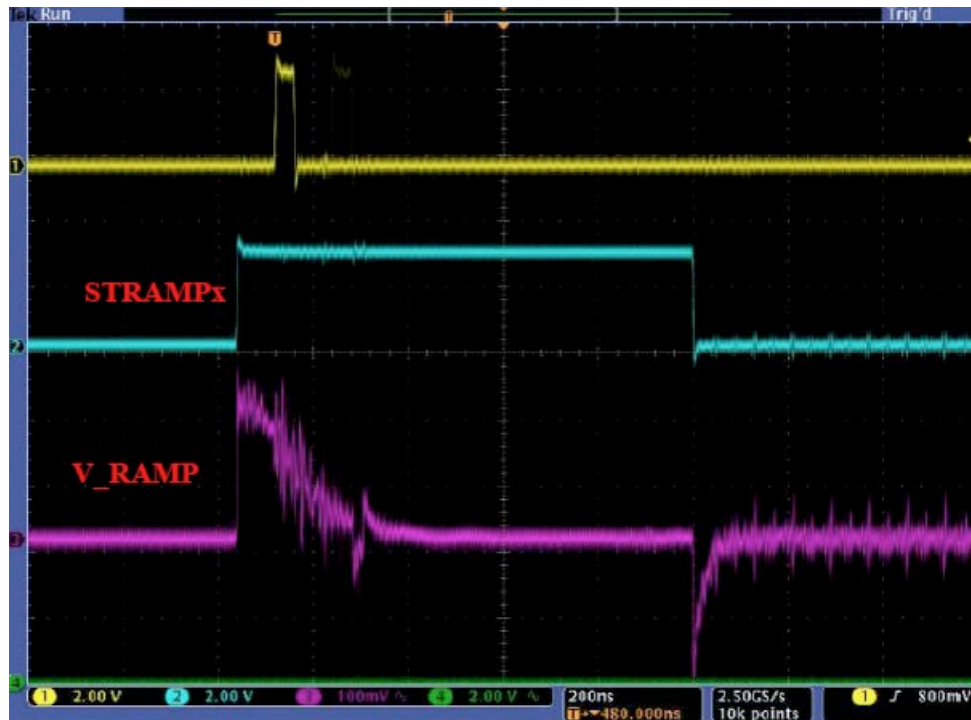


Fig. 15 V_RAMP voltage after mounting 1.1 kohm resistor to ground.

3.3. Voltage Signals

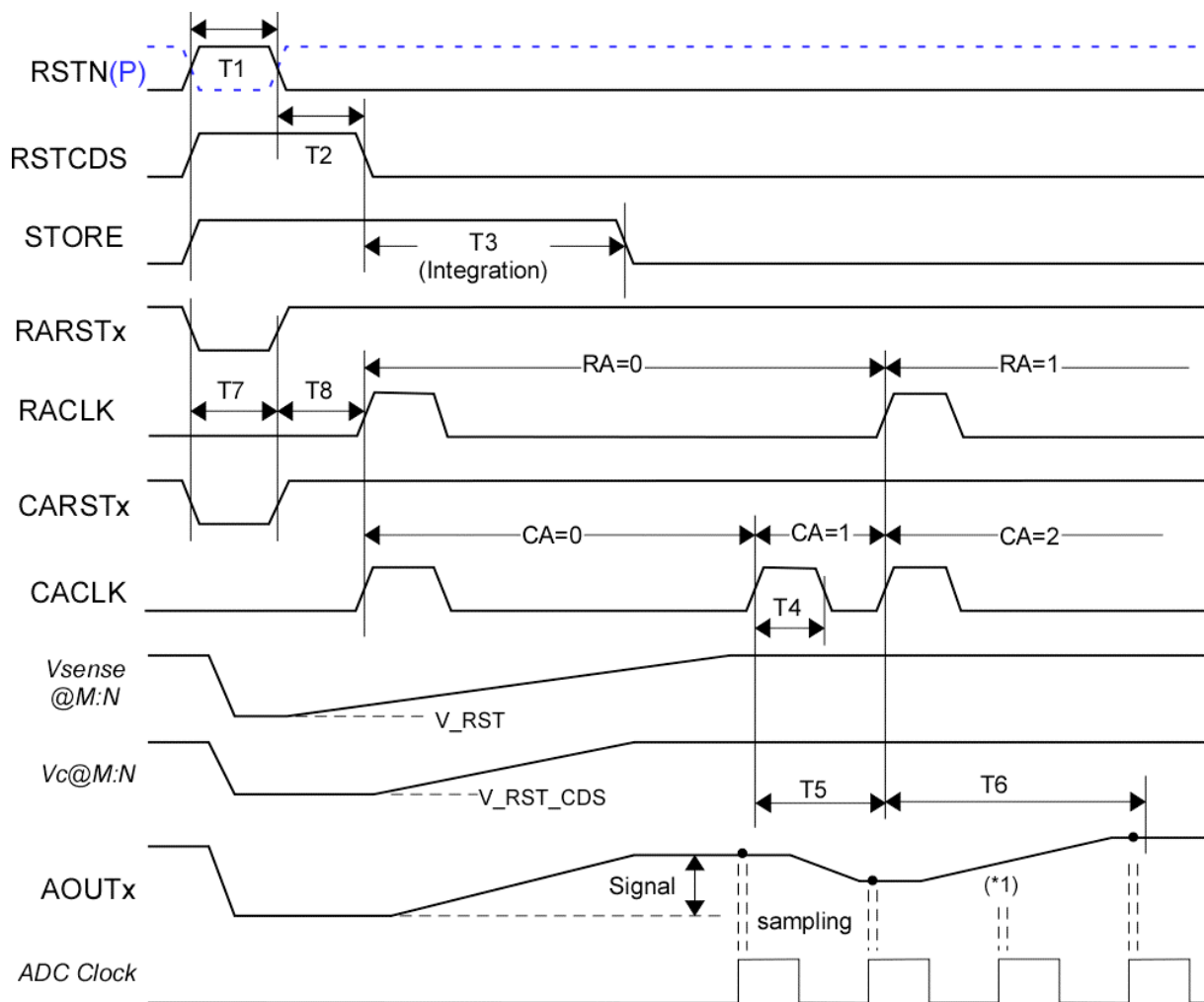
- VDD33
Power supply voltage for 3.3V I/O.
- VDD18
Power supply voltage of 1.8V core circuit.
- VSS
Ground connection.
- VDET
Sensor bias voltage supplied from HV Ring on the top.
- VBACK
Sensor bias voltage supplied from back side of chip.
- VBIAS
BIAS Ring voltage (outermost p-type ring). This line is also connected to BPW under I/O buffers and peripheral circuits.

3.4. Data I/O Timing

CDS 付き AOUTx の出力タイミングを Fig. 16 に示す。この読み出しでピクセル内トランジスタ P1 及び kTC ノイズに相当する電圧は、ピクセル出力から差し引かれるが、P3 及び Column buffer による offset はまだ差し引かれない。この影響も差し引く為には、あらかじめ?に示すようなタイミングで各ピクセルの offset 電圧を読み出ししておき、Fig. 16 で得られたデータから差し引く必要がある。

Fig. 17 is timing diagram used in Piotr Kapusta's test, and Fig. 18 shows scope display at that time.

[AOUTx sampling timing]



(*1)Skip the data in this cycle when the clock period is shorter than T6.

Fig. 16 Sampling timing of the analog output (AOUTx) signals.

Table 1 Readout timing value in the analog output. Very Preliminary!

Symbol	Characteristics	Min	Max	Unit	Comment
T1	RST width	10		ns	
T2	RSTCDS overhang	10		ns	
T3	STORE overhang	10		ns	
T4	CACLK(RACLK) width	10		ns	
T5	Column Address change to AOUTx valid (CACLK width)	100		ns	
T6	Row Address change to AOUTx valid (RACLK width)	200		ns	T5 > T4
T7	CARSTx(RARSTx) width	10		ns	
T8	CARSTx(RARSTx) negate to CACLK(RACLK) time	10		ns	

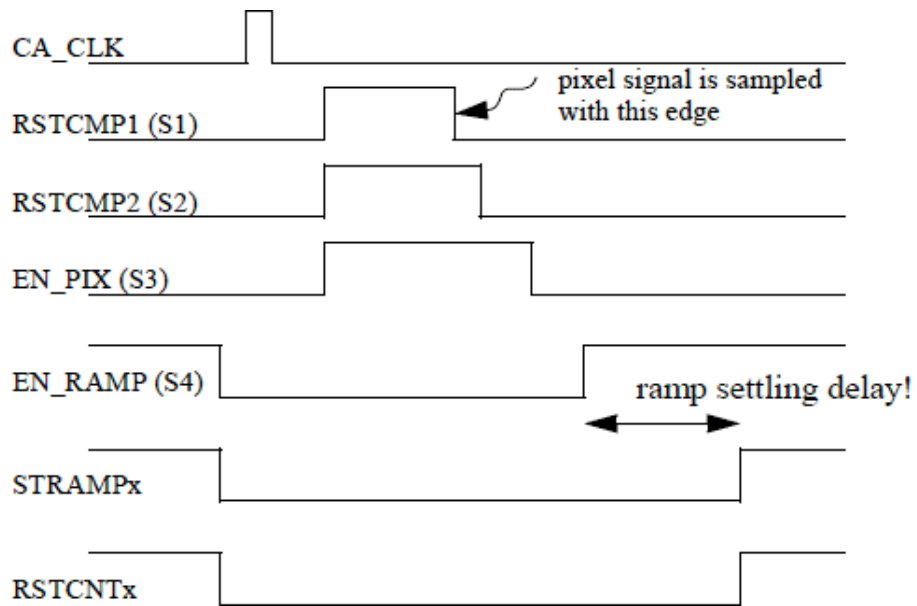


Fig. 17 Sequence of the column ADC control signal.



Fig. 18 Scope image of the column ADC control signal.