



# SOI Monolithic Pixel Detector Technology

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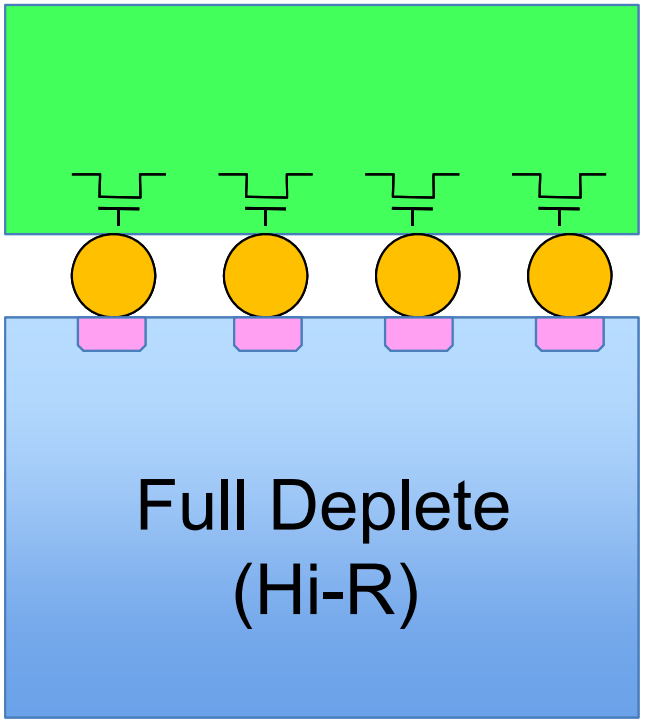
# Outline

I. Introduction
II. Recent Progress
*Double SOI Wafer & Process
*Higher Dose LDD
*Layout Shrinking with NMOS-PMOS merge
III. Examples of SOI Detectors
IV. Summary

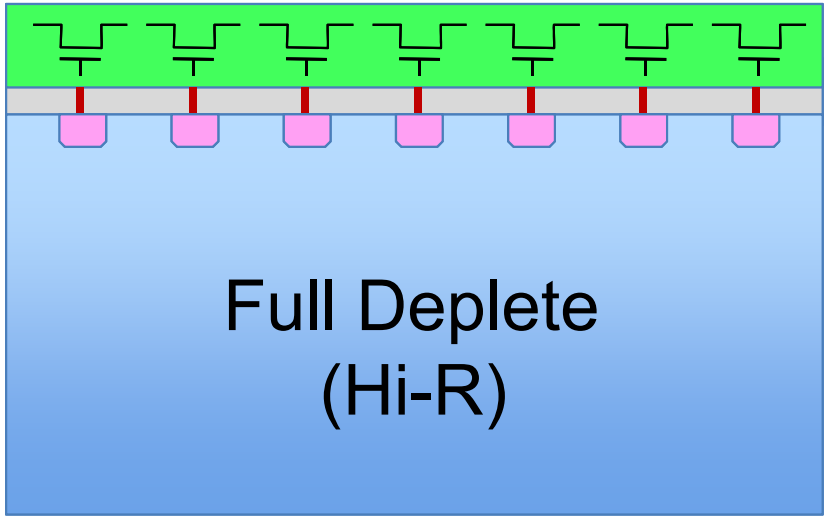
Poster Presentations
- 'A monolithic pixel sensor with fine space-time resolution based on silicon-on-insulator (SOI) technology for the ILC vertex detector', S. Ono, et al.

# I. Introduction

Hybrid Detector



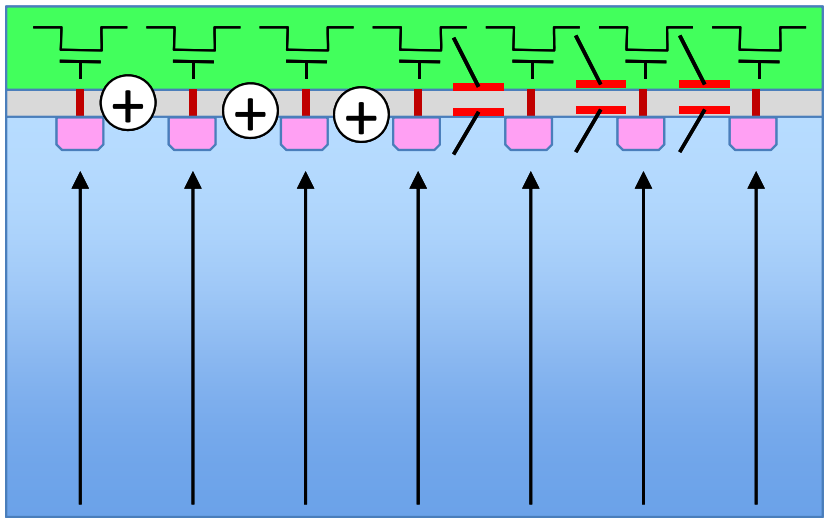

Silicon-On-Insulator (SOI)




To use SOI technology for pixel detector is already discussed in 1990(*).

(*) Jean-Pierre Colinge, 'An overview of CMOS-SOI technology and its potential use in particle detection systems', NIM A305 (1991) 615-619.

# Issues in SOI Pixel



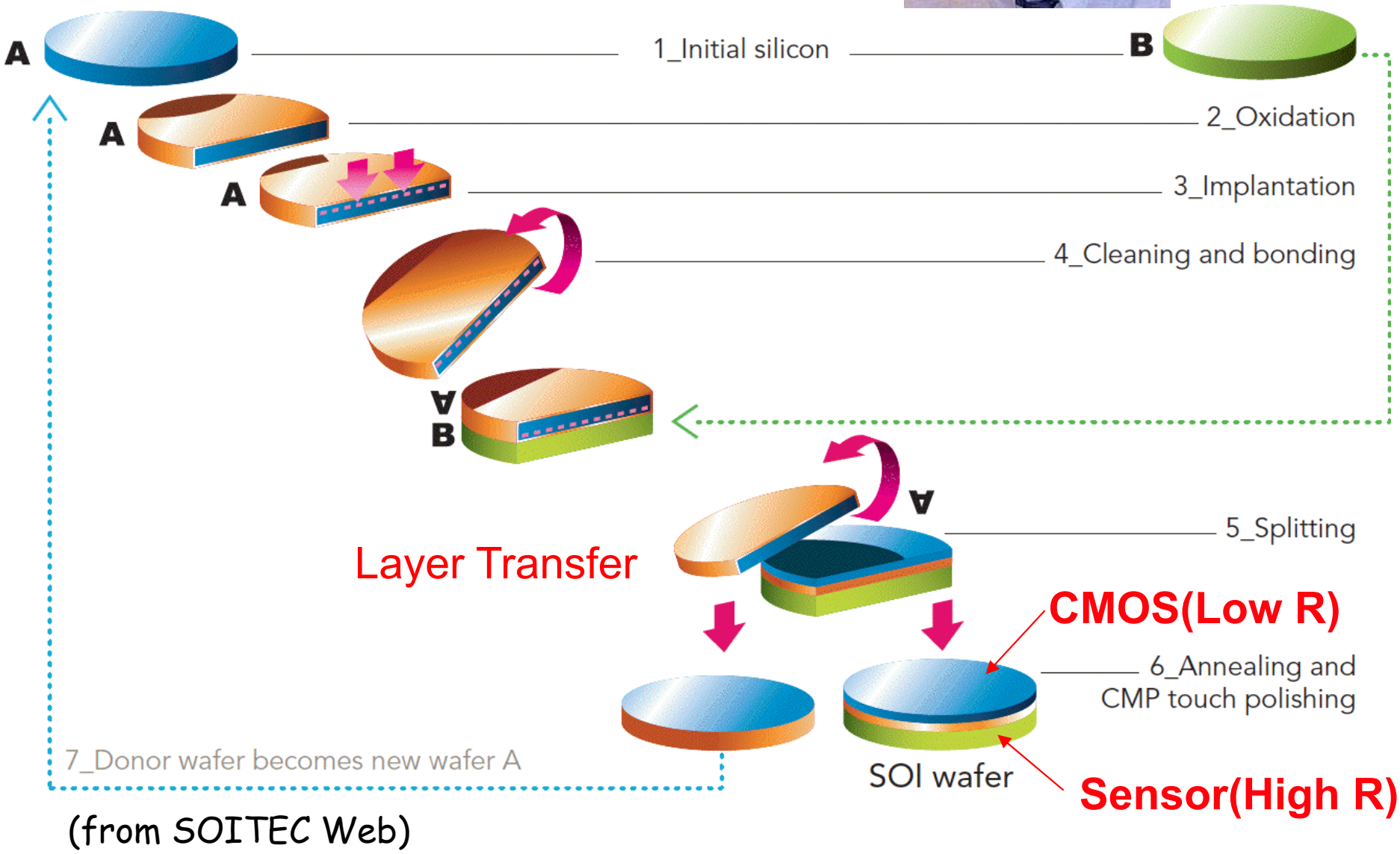

- Transistors does not work with Detector High Voltage. (Back-Gate Effect)
- Circuit signal and sense node couples. (Signal Cross Talk)
- Oxide trapped hole induced by radiation will shift transistor threshold voltage. (Radiation Tolerance)

Unfortunately, in 1990s, due to immature process technology, no good high-resistivity SOI wafer etc. , many SOI sensor R&D projects were stopped.

# SmartCut (1991)

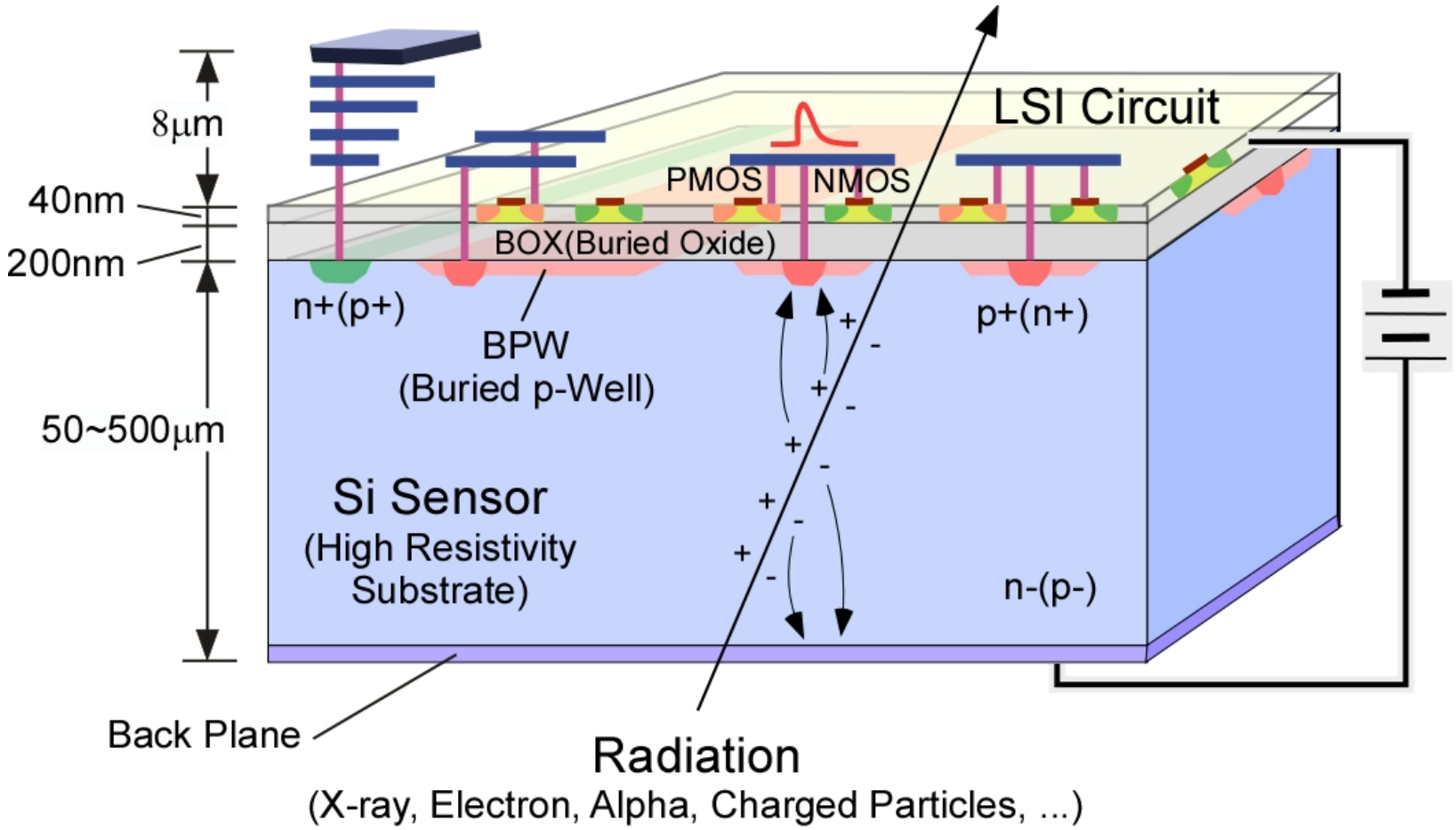
Michel. Bruel (Leti)

Become popular after 2000 (SOITEC Co.).



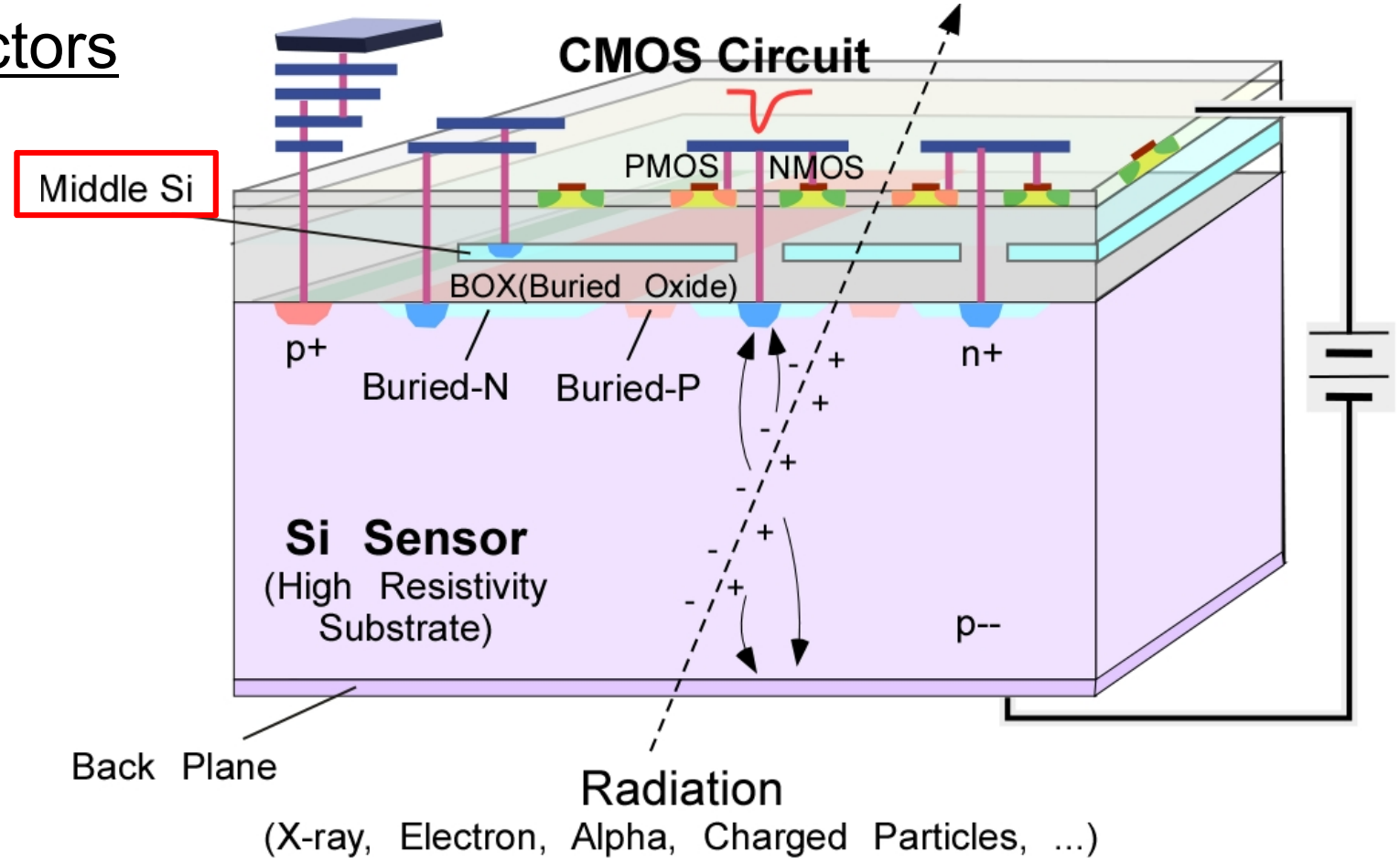

(from SOITEC Web)

# SOIPIX Detector (Single)




Single SOI Detector
- Buried-Well shield back-gate potential
- Good for Integration-type sensor
- Relatively Low radiation applications

# SOIPIX Detectors (Double)

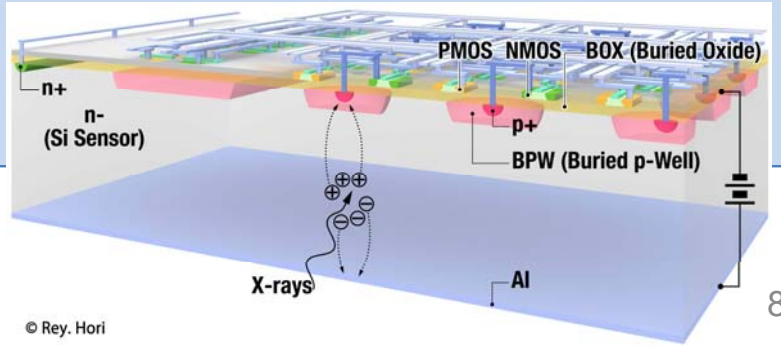



Double SOI Detector

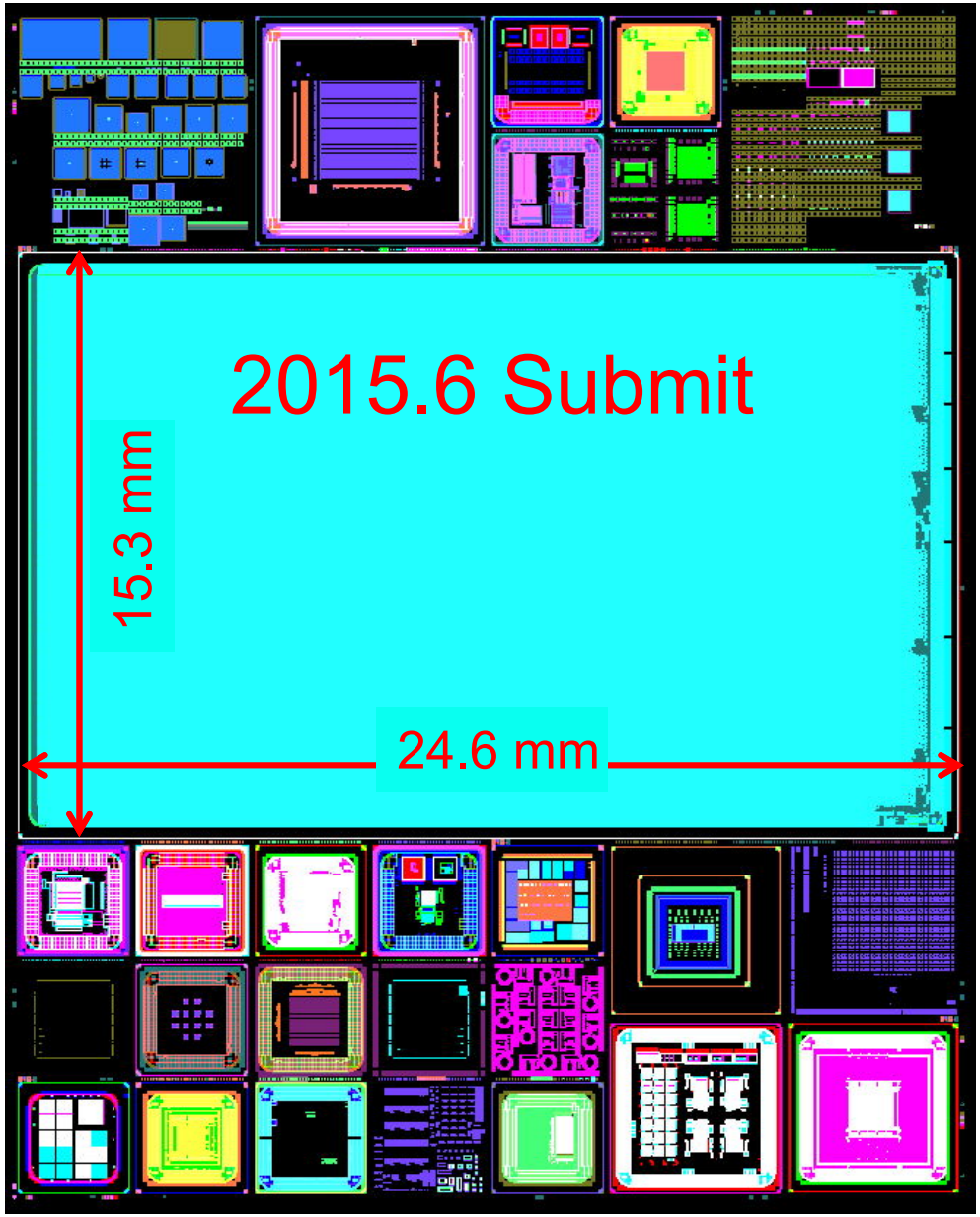
- Middle Si layer shields coupling between sensor and circuit.
- It also compensate E-field generated by radiation trapped hole.
- Good for Complex function and Counting-type sensor.
- Can be used in High radiation environment.

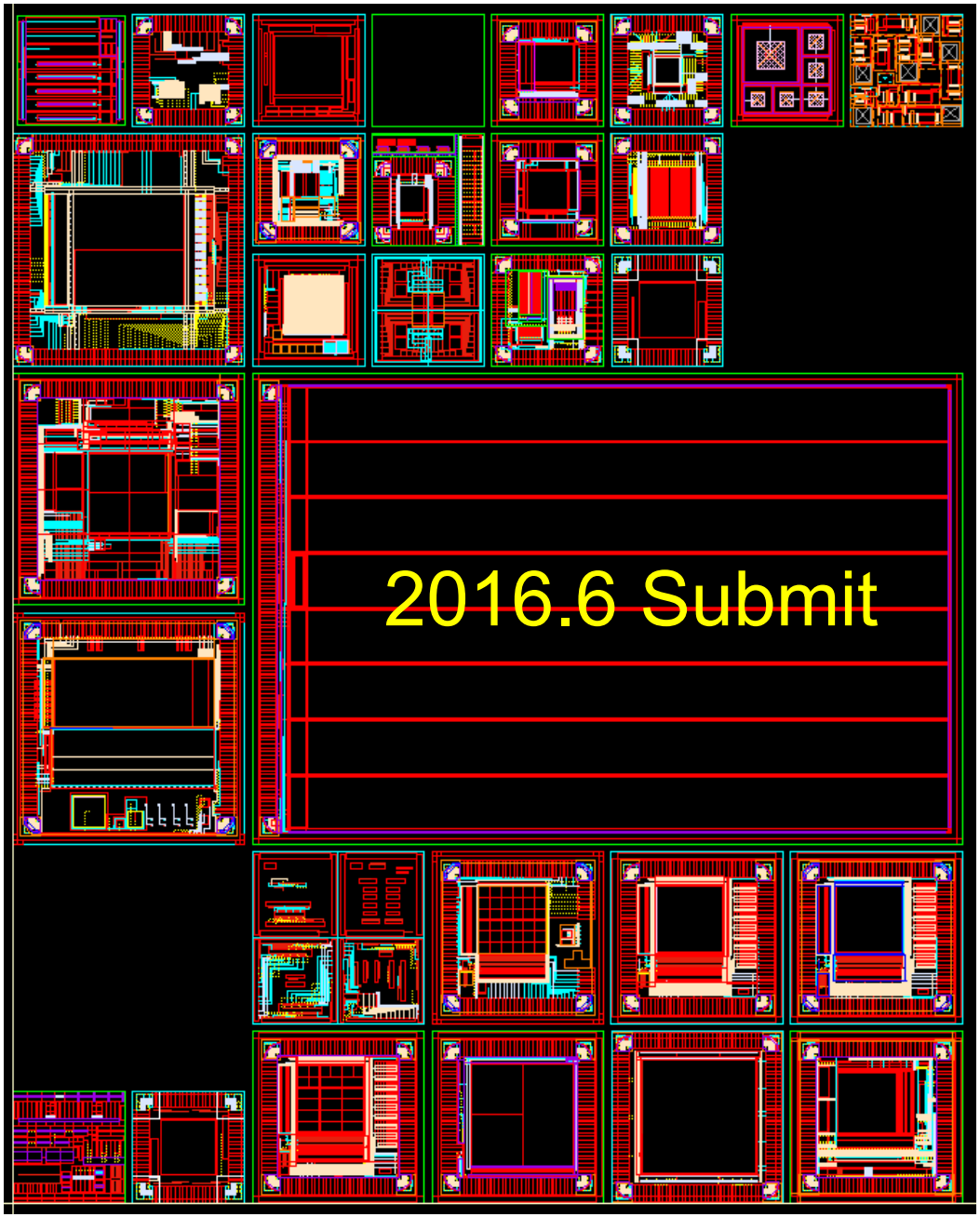
# Features of SOI Pixel Detector

- Monolithic device. No mechanical bonding.
- Fabricated with semiconductor process only.
  → High reliability and Low Cost.
- High Resistive fully depleted sensor (50um~700um thick) with Low sense node capacitance. → Large S/N.
- On Pixel processing with CMOS circuits.
- No Latch up and very low Single Event cross section.
- Can be operated in wide temperature (1K-570K) range.
- Based on Industry Standard Technology.



KEK SOI Multi-Project Wafer run. (1~2 runs/year)



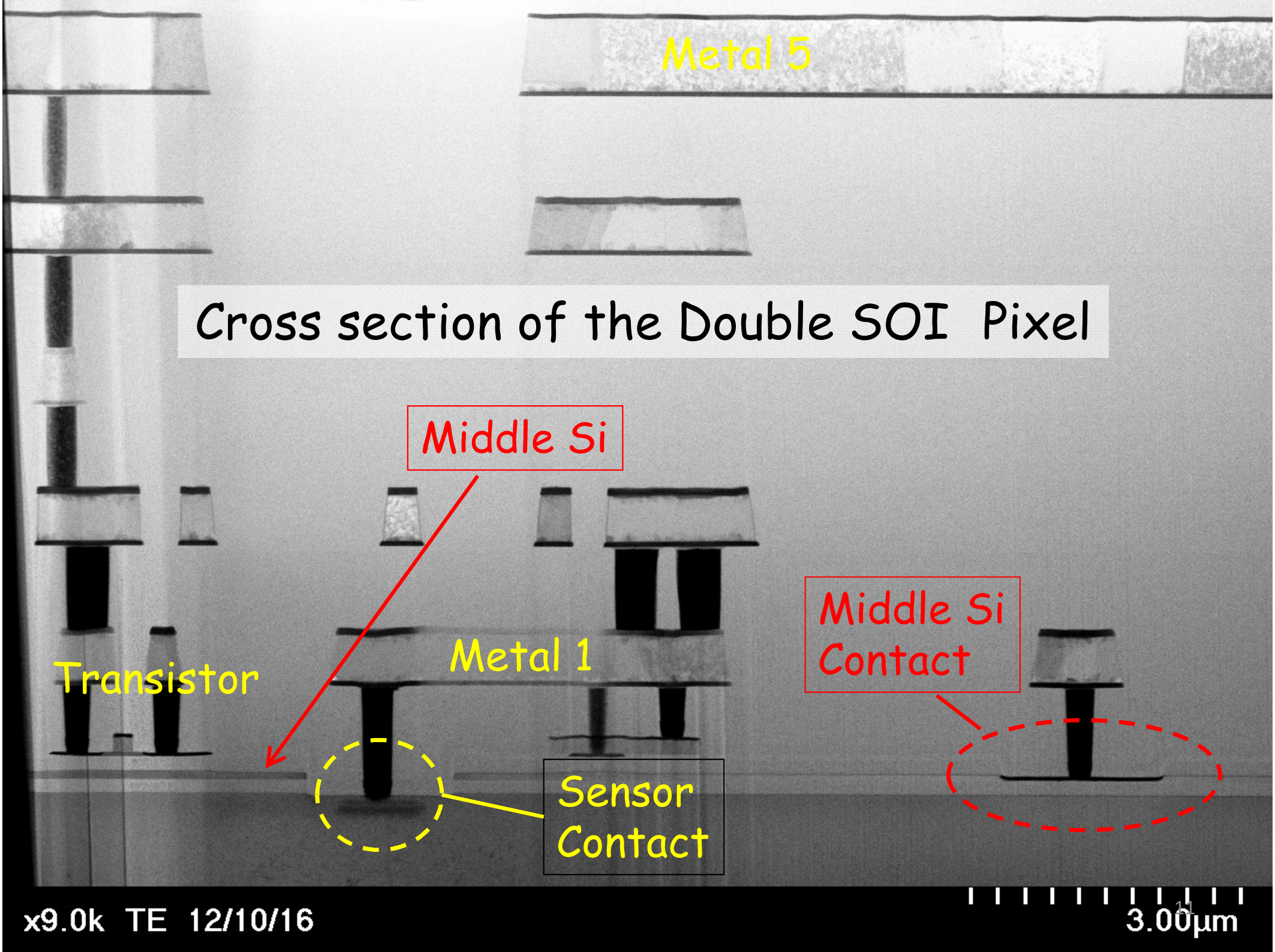



# II. Recent Progress

***Double SOI Wafer & Process**

***Higher Dose LDD**

***Layout Shrinking with NMOS-PMOS merge**

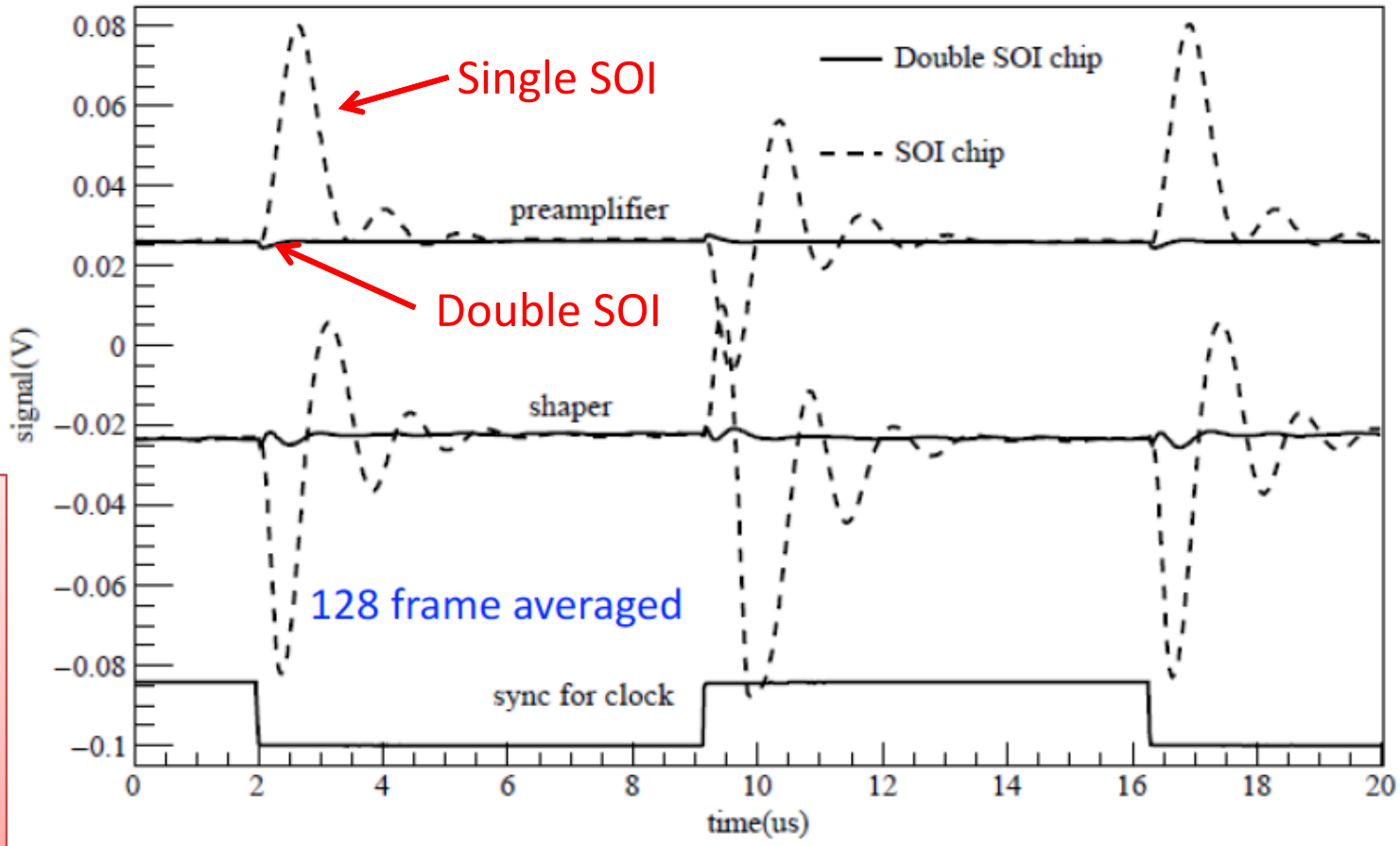

Metal 5
Cross section of the Double SOI Pixel
Middle Si
Transistor
Metal 1
Middle Si
Contact
Sensor
Contact
x9.0k TE 12/10/16
3.00µm

# Specification of Double SOI wafer

| Layer | Present Lot | Next Lot |
|---|---|---|
| SOI1 | p-type 88 nm,<br>< 10 Ω •cm | p-type 88 nm,<br>< 10 Ω •cm |
| BOX1 | 145 nm | 145 nm |
| SOI2 | n-type 150 nm,<br>< 10 Ω •cm | n-type 150 nm,<br>3-5 Ω •cm |
| BOX2 | 145 nm | 145 nm |
| Substrate | p-type<br>Low Oxygen Cz, 725um,<br>> 1.0 k Ω •cm | p-type<br>FZ, 725um,<br>> 5.0 k Ω •cm |

# Effect of Double SOI

## Cross Talk from Clock line

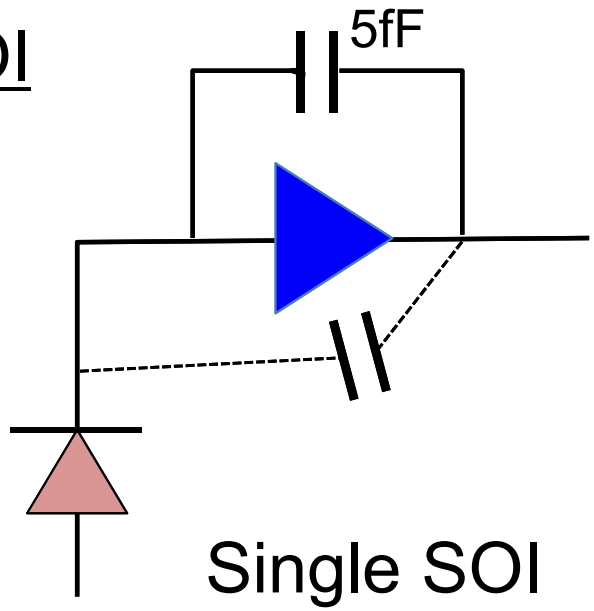



(by Lu Yunpeng (IHEP))

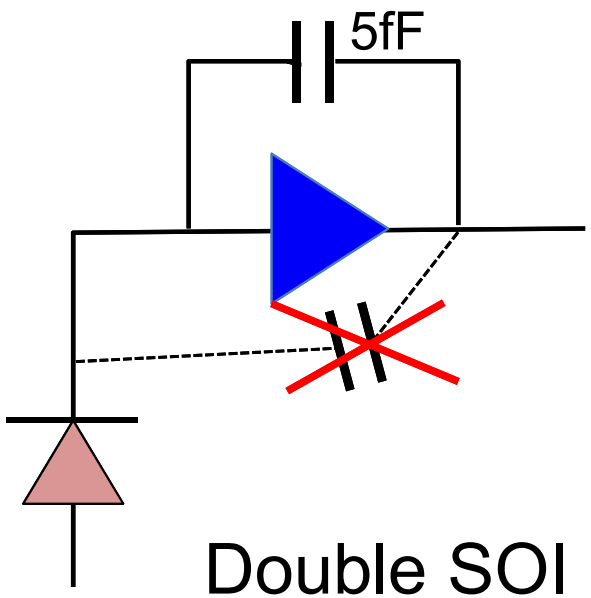
Shield:
Cross Talk between Circuit and Sensor is reduced to 1/20.

# Effect of Double SOI

Coupling:
Gain of Charge Amp increases ~3 times by cutting parasitic C.

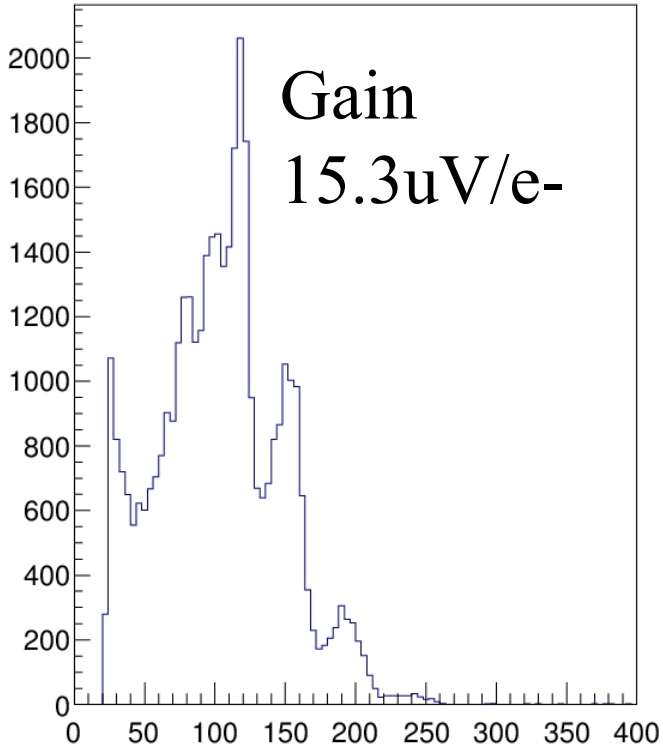


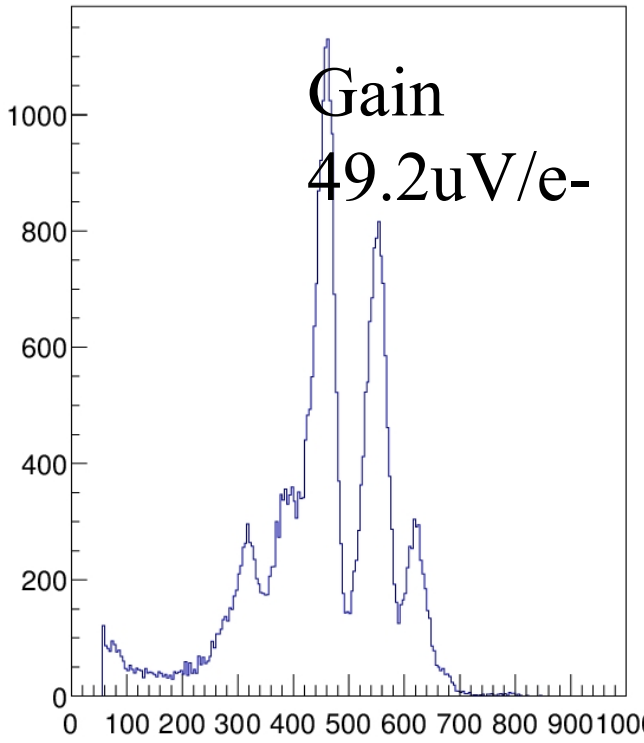

Single SOI




Double SOI

Am241

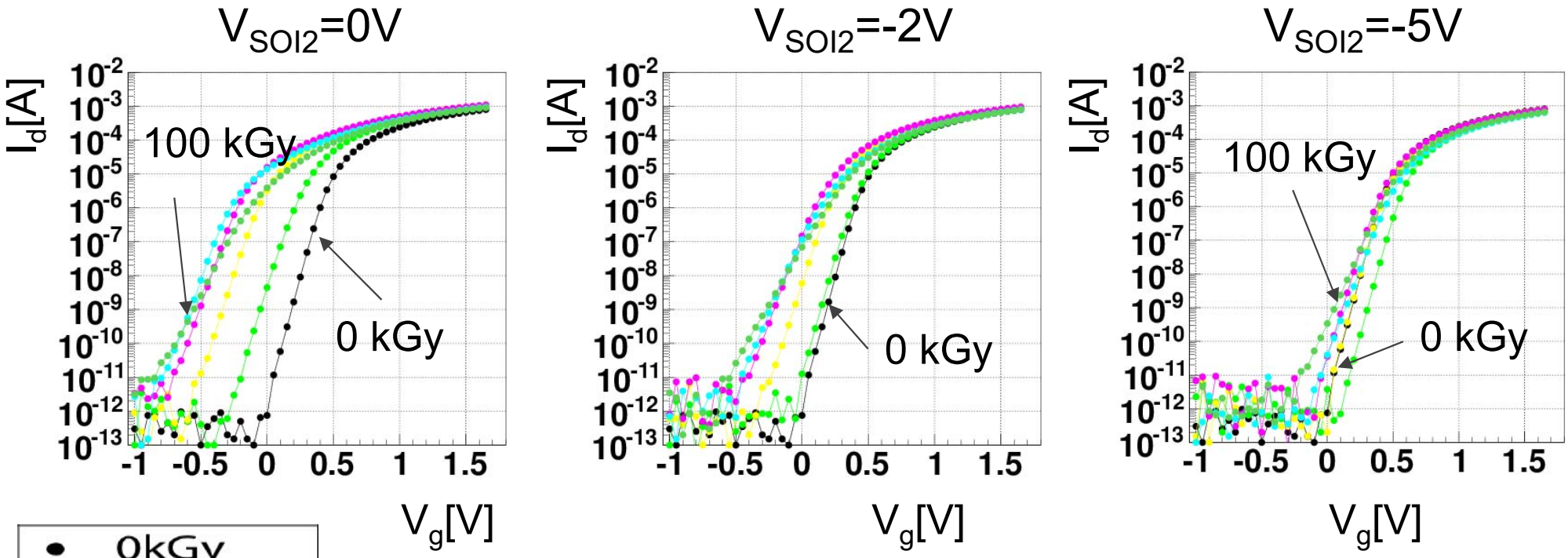


# Gamma-ray Irradiation Test
## (Id-Vg Characteristics v.s. SOI2 Potential)

I/O normal Vth
Source-Tie Tr.
L/W =0.35um/5um

**NMOS**




By setting Middle Si potential (Vsoi2) to -5V, Id-Vg curve returned nearly to pre-irradiation value at 100 kGy(Si) (10 Mrad).

(by U. of Tsukuba)

*Double SOI Wafer & Process

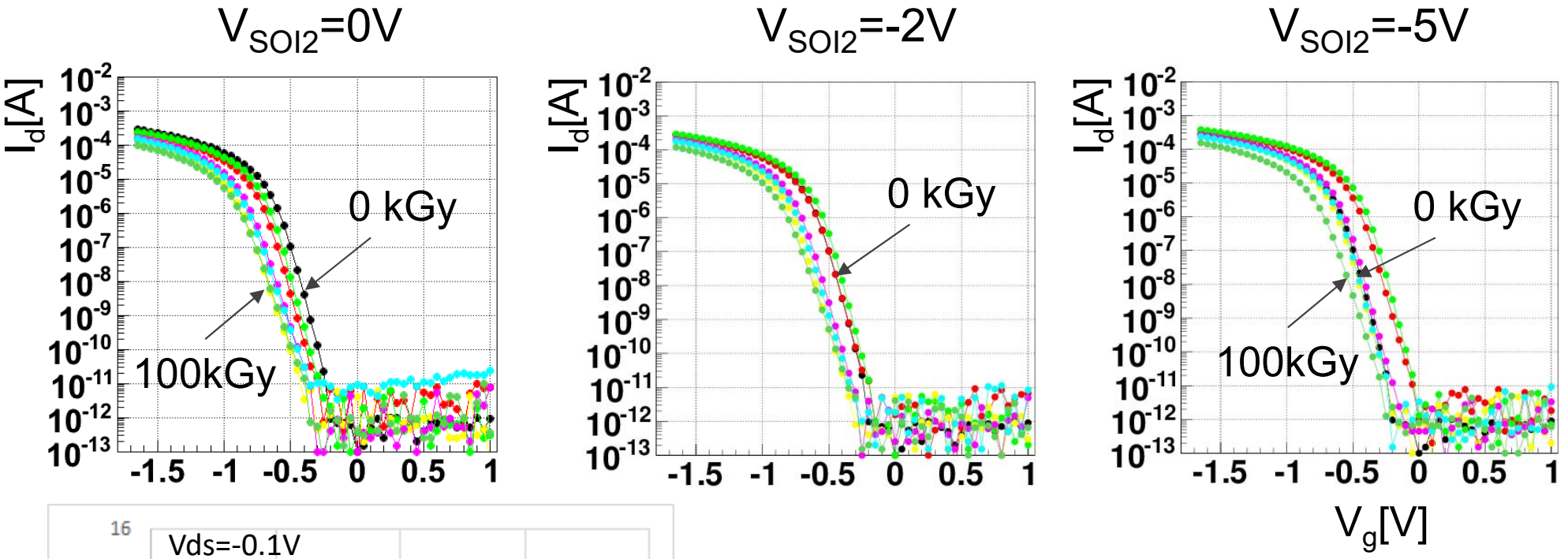
*Higher Dose LDD

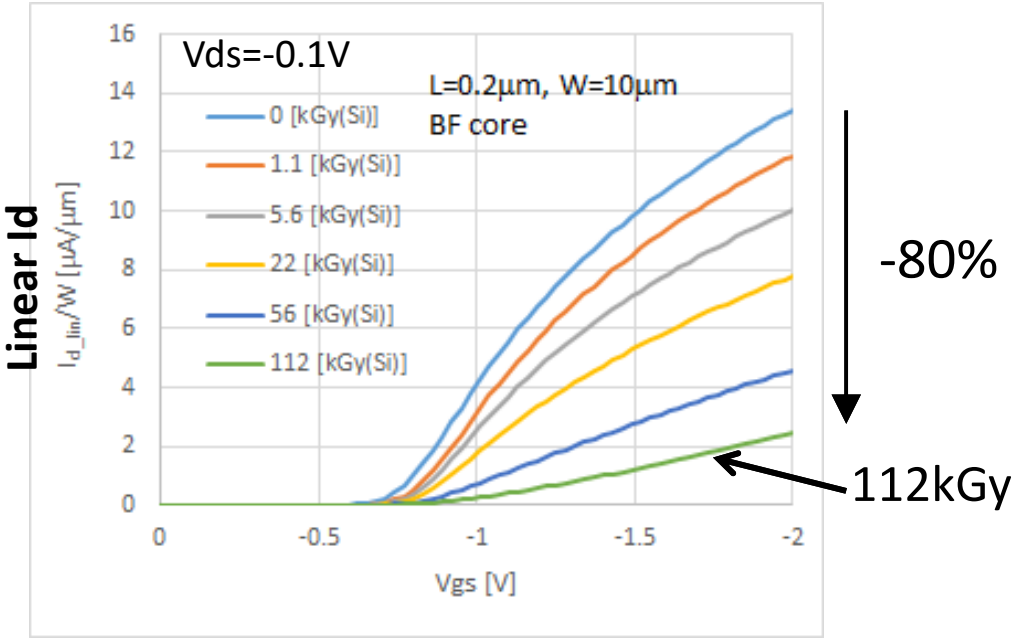
*Layout Shrinking with NMOS-PMOS merge

# Variation of Id-Vg Characteristics and Effect of SOI2 Potential

**PMOS**

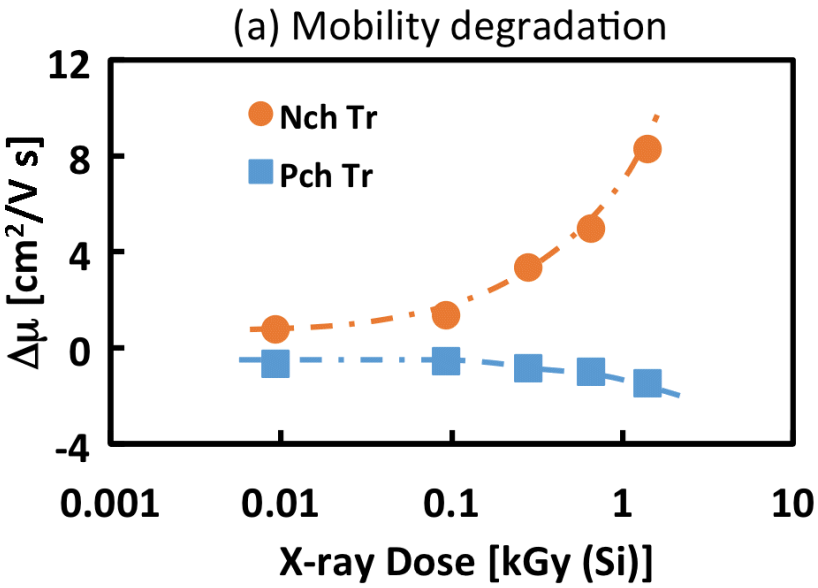
I/O Normal Vt
Source-Tie
L/W =0.35um/5um

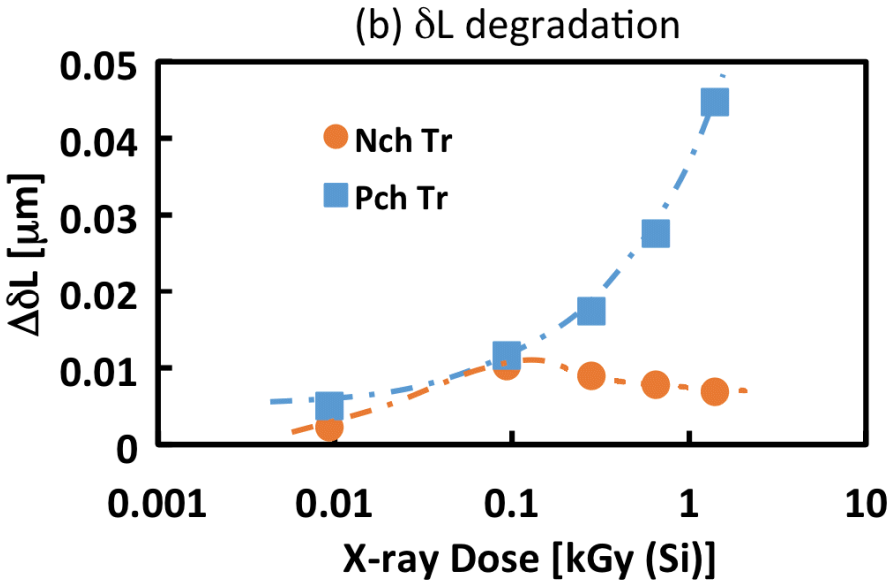


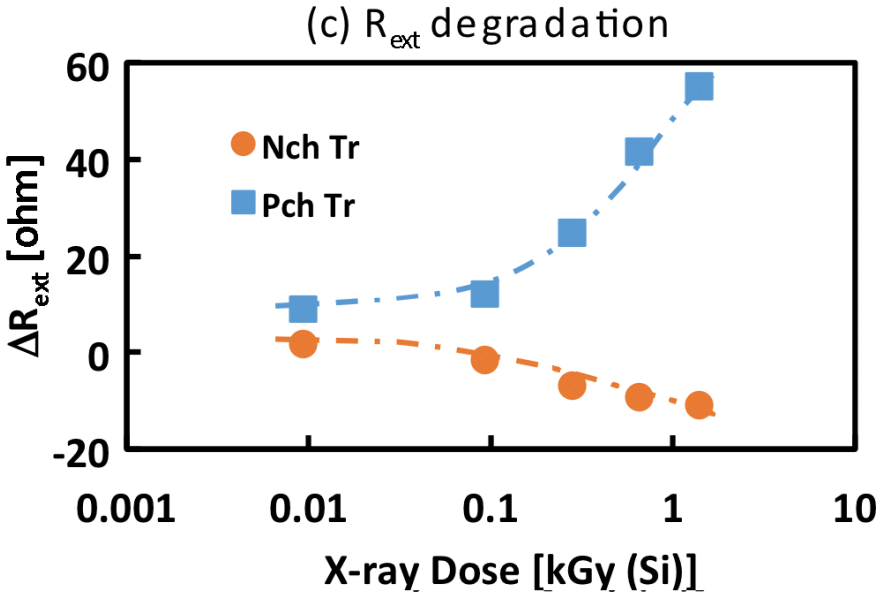




Threshold voltage shift is not so large in PMOS, but Drain Current decreases much .

# Radiation Effect to NMOS & PMOS



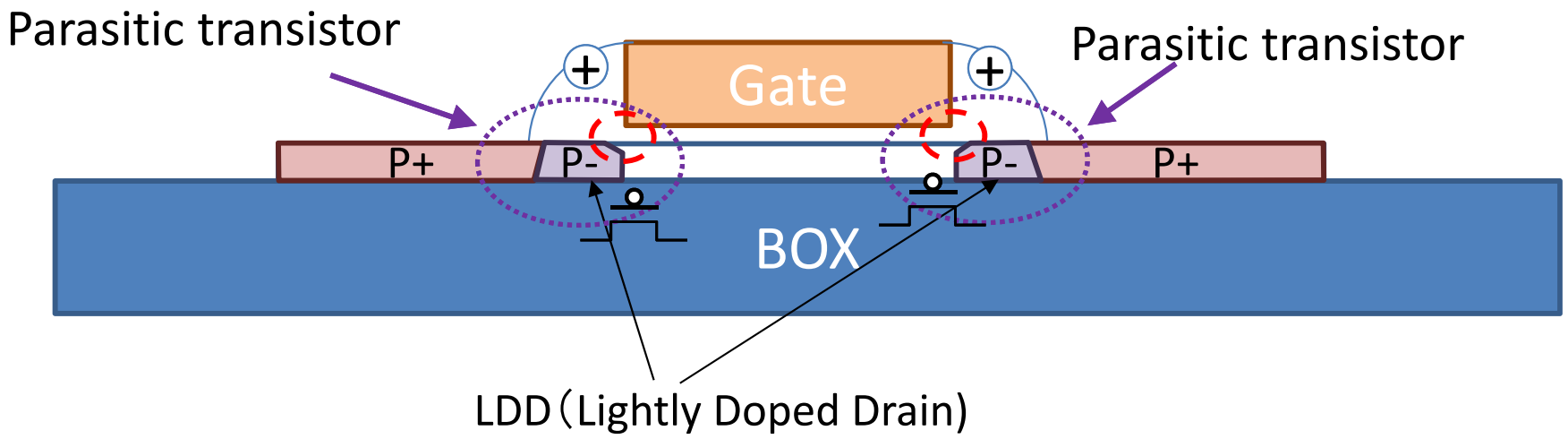




In PMOS, effective Gate Length become longer and Channel Resistance is increased with radiation.

→ Radiation Induced Gate LEngth Modulation (RIGLEM).

# Dose Increase in Lightly Doped Drain (LDD) Region

- Major cause of the drain current degradation by radiation is Vth increase at gate edge due to positive charge generation in spacer.
- Charge in spacer control the Vth of the parasitic transistor.
- To reduce this effect, lightly doped drain (LDD) dose should be increased.
- Present process has rather low dose in LDD region to aiming lower power.



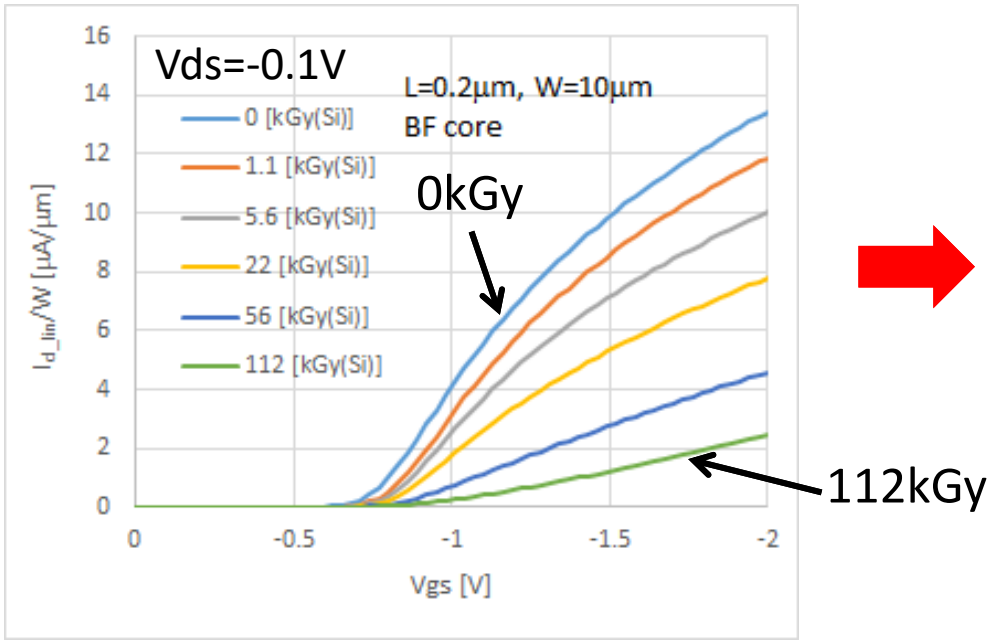

(by I. Kurachi)

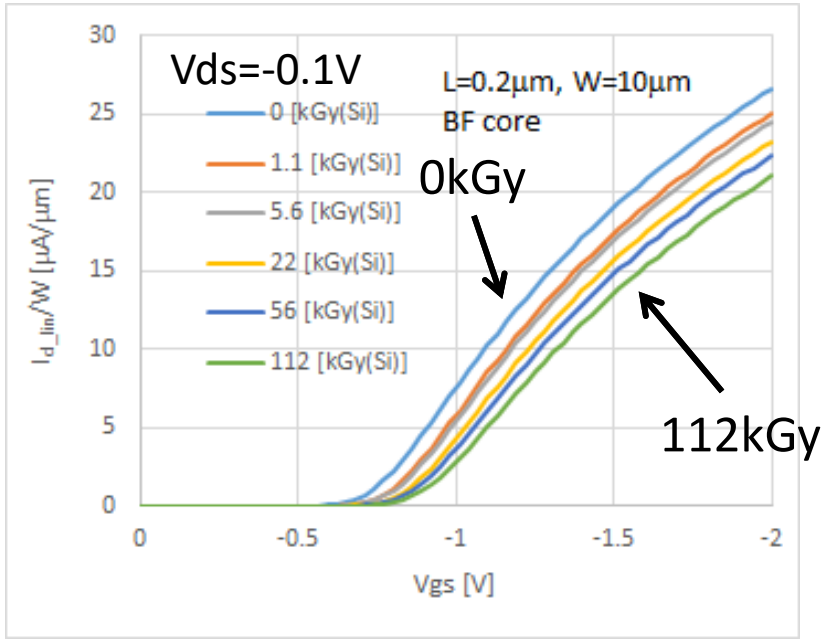
# Id-Vg Characteristics in Triode Region

Present Process

LDD Dose x 6

Linear Id




With increasing Implantation dose of PLDD region 6 times higher than present value, the degradation is reduced from 80% to 20% at 112 kGy(Si).

Ref.) I. Kurachi, et al. "Analysis of Effective Gate Length Modulation by X-Ray Irradiation for Fully Depleted SOI p-MOSFETs, IEEE Trans. on Elec. Dev. Vol. 62, Aug. 2015, pp. 2371-2376.

*Double SOI Wafer & Process

*Higher Dose LDD

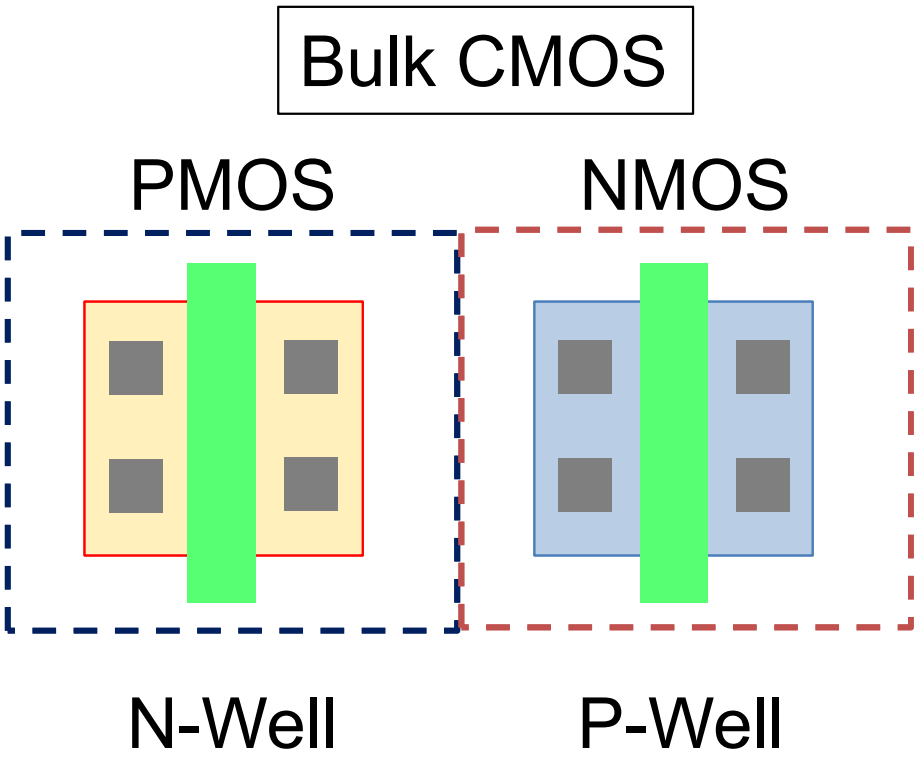
*Layout Shrinking with NMOS-PMOS merge

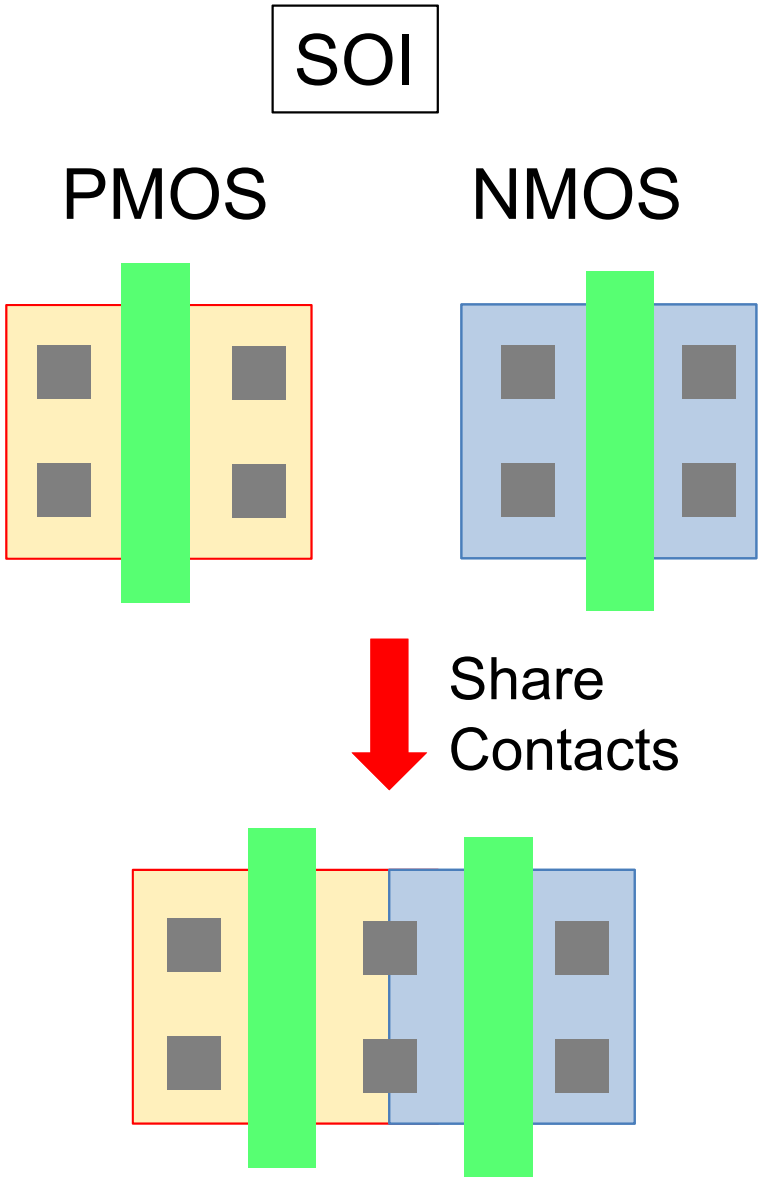
# Lapis Semi.(*) 0.2 μm FD-SOI Pixel Process

| | |
|---|---|
| Process | 0.2μm Low-Leakage Fully-Depleted SOI CMOS<br>1 Poly, 5 Metal layers.<br>MIM Capacitor (1.5 fF/um$^2$), DMOS<br>Core (I/O) Voltage = 1.8 (3.3) V |
| SOI wafer | Diameter: 200 mmϕ, 720 μm thick<br>Top Si : Cz, ~18 Ω-cm, p-type, ~40 nm thick<br>Buried Oxide: 200 nm thick<br>Handle wafer: Cz (n) ~700 Ω-cm,<br>FZ(n) > 2k Ω-cm, FZ(p) ~25 k Ω-cm etc. |
| Backside process | Mechanical Grind, Chemical Etching, Back side Implant, Laser Annealing and Al plating |

(*) Former OKI Semiconductor Co. Ltd.

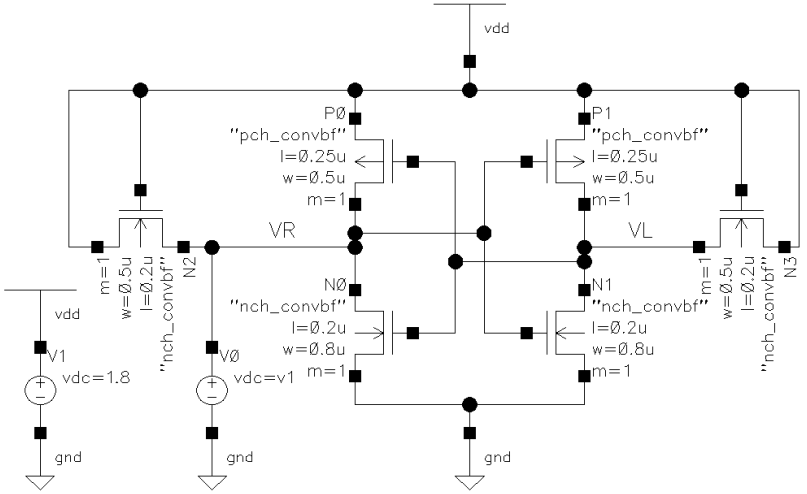
# Layout Shrink（Active Merge)

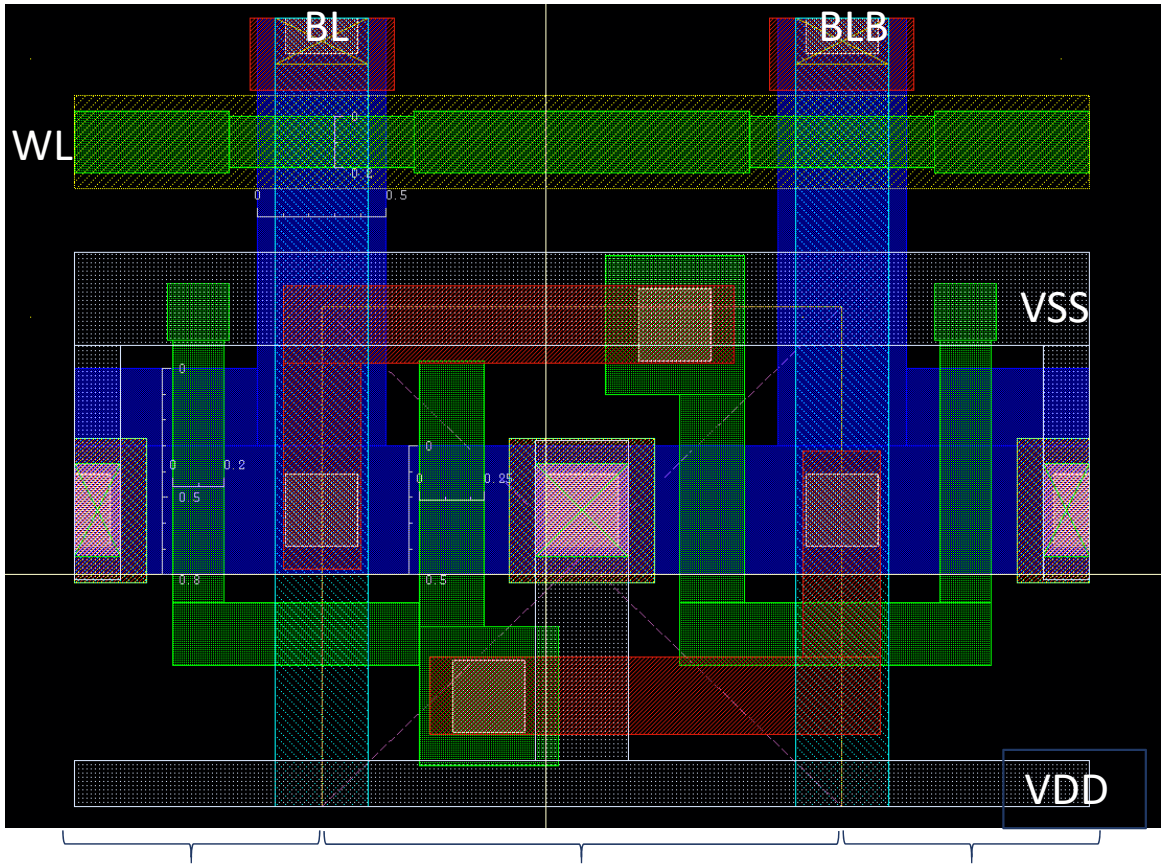



In the SOI process, it is possible to merge NMOS & PMOS Active region and share contacts.

# Single Port SRAM Bit Cell

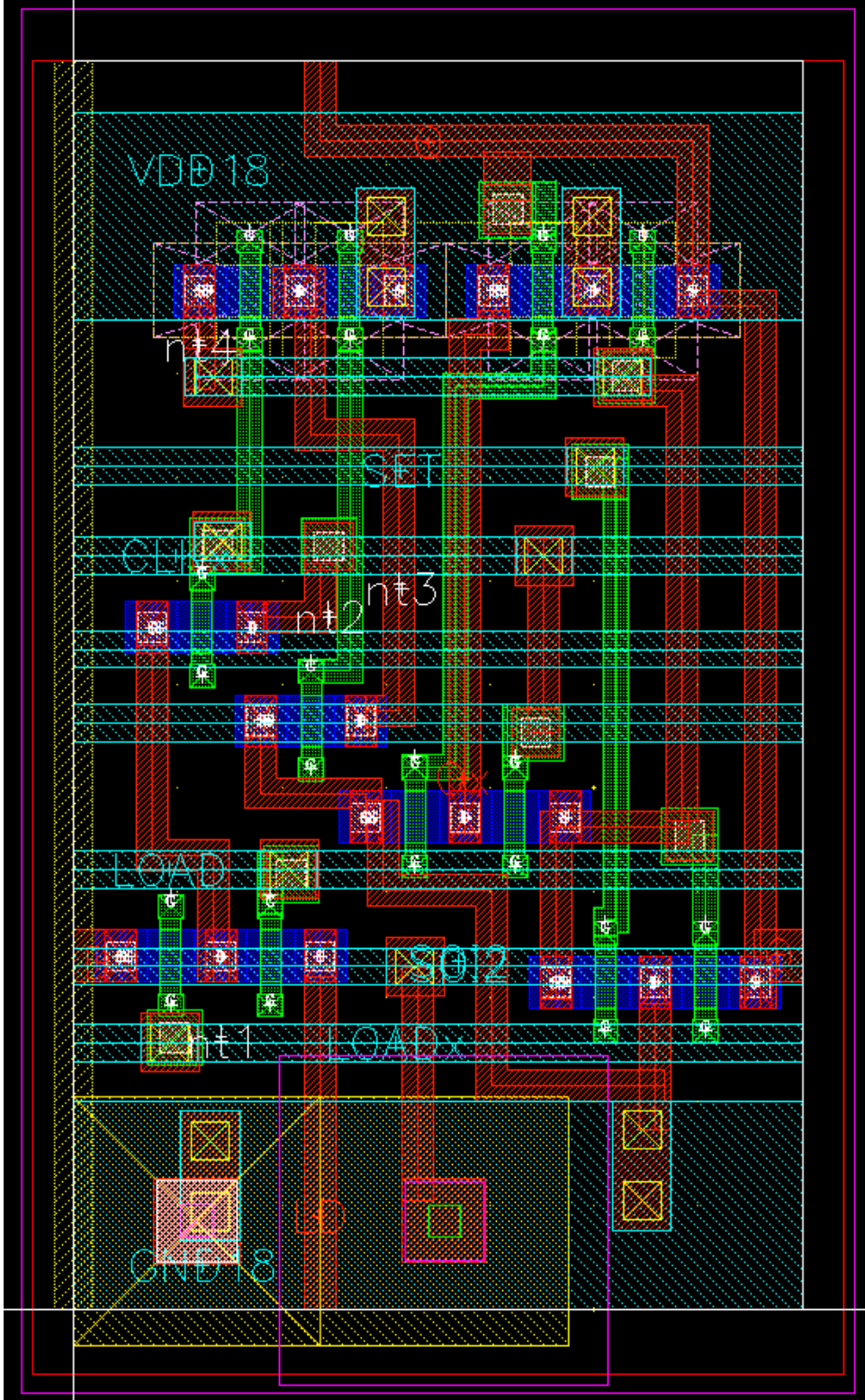



Only 1 Active region

Nch Pch Nch

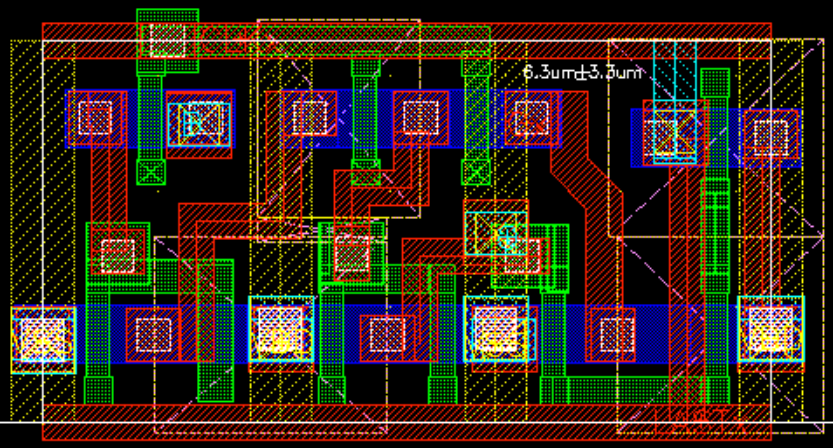
Cell Size : 3.94µm X 3.06µm = 12.06µm²



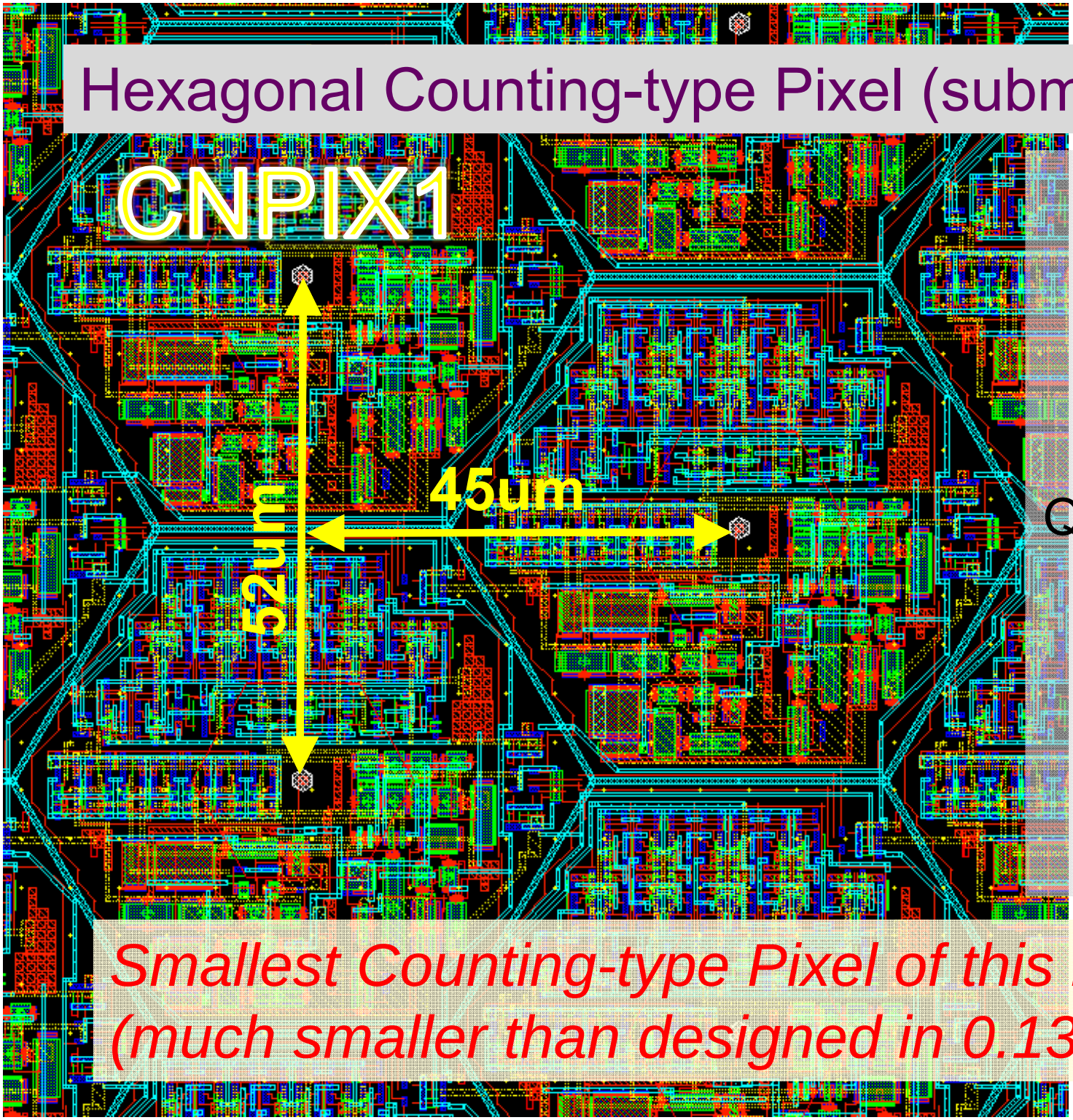

12x7=84um2

New D Flip-Flop
25% of Previous Cell

3.3x6.3=20.79um2



# Hexagonal Counting-type Pixel (submitted in June)

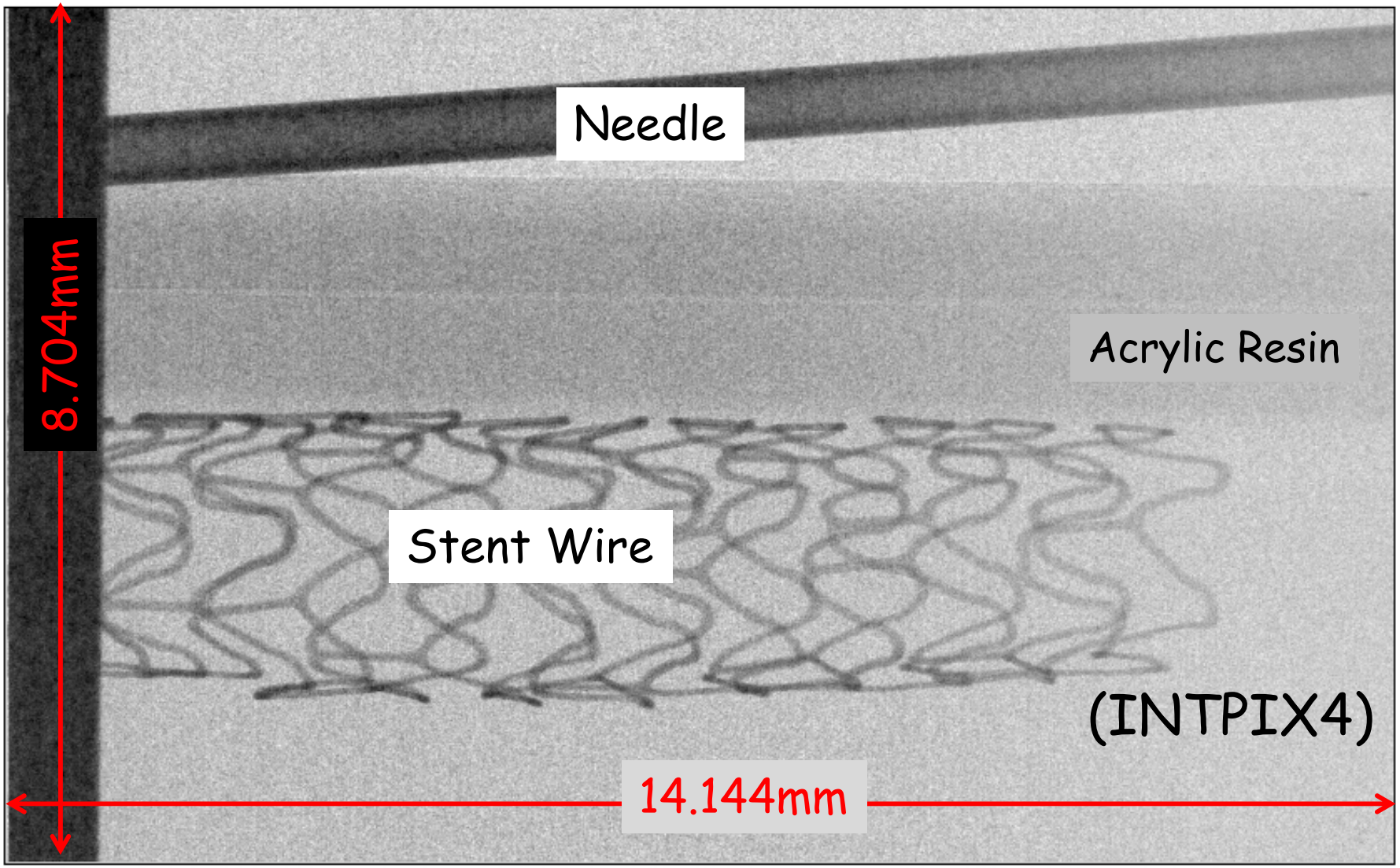



Charge Amp
+
Shaper
+
Discriminator
+
Q Share Handling
+
19bit Counter
+
7bit register

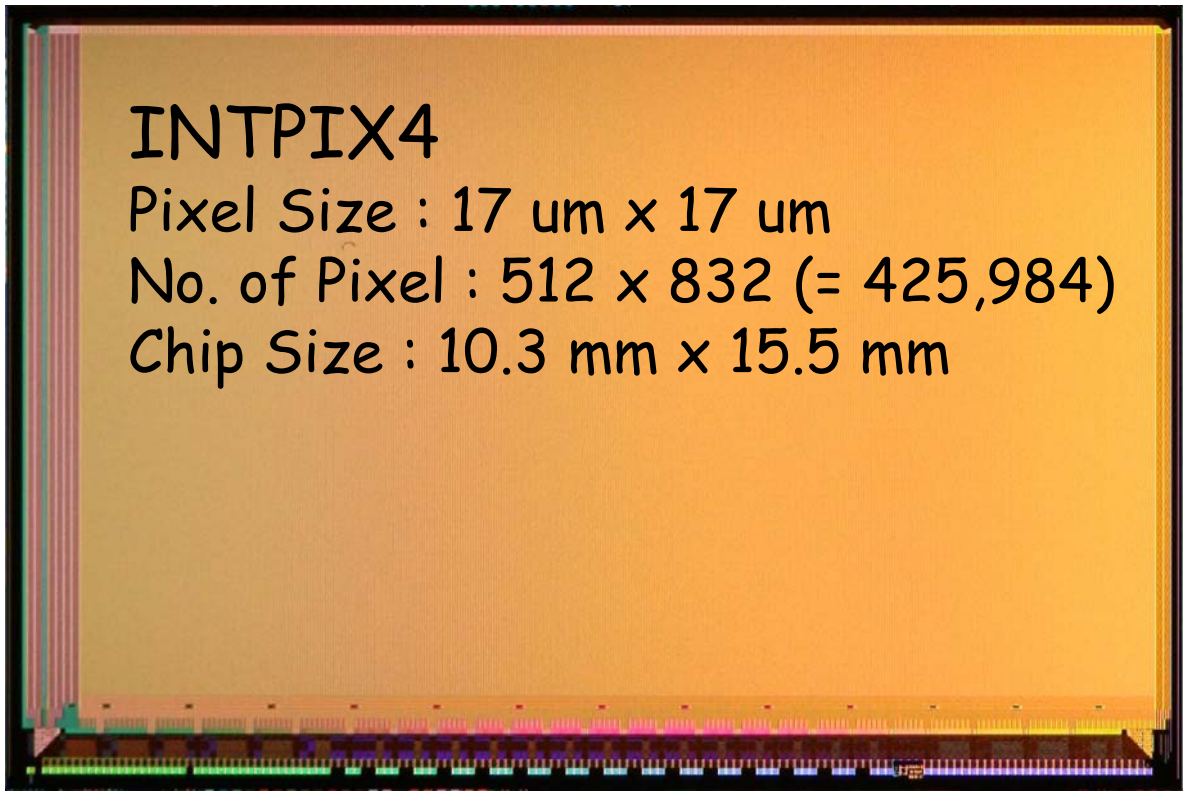
(in 2,340 $um^2$)

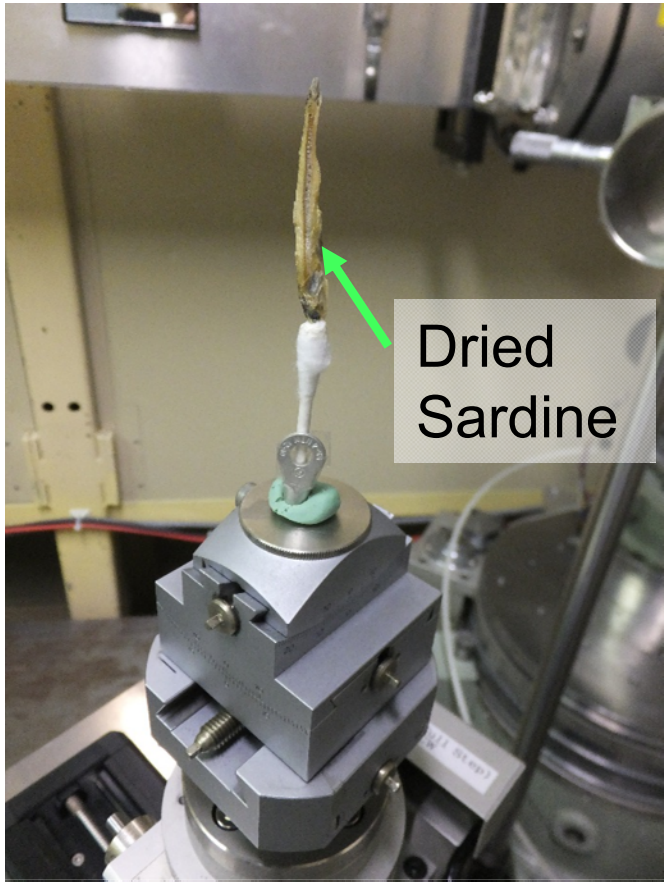
*Smallest Counting-type Pixel of this kind.*
*(much smaller than designed in 0.13um process)*

# III. Examples of SOI Detectors



# Integration type detector & 3D CT




- Sensor : INTPIX4 FZn, Backside Illumination
- HV : 200V、Integration Time : 1ms、ScanTime : 320ns/pix, 1000frame/event
- KEK PF, X-ray Energy : 9.5keV
- Took images for 0~180° at every 1 degree.

(by R. Nishimura, K. Hirano (KEK)

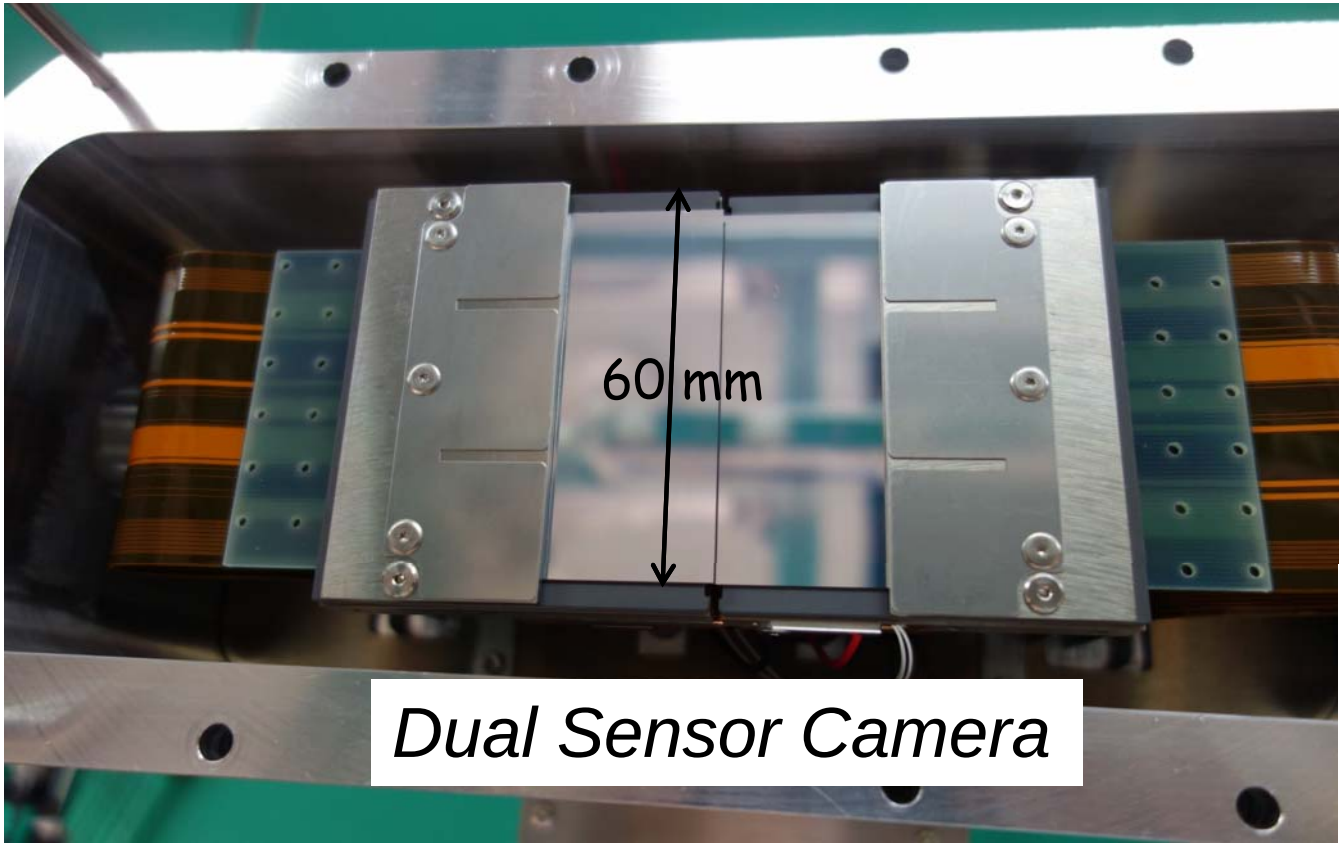
# INTPIX4: Computed Tomography with Syncrotron X-ray


(by R. Nishimura, K. Hirano (KEK)

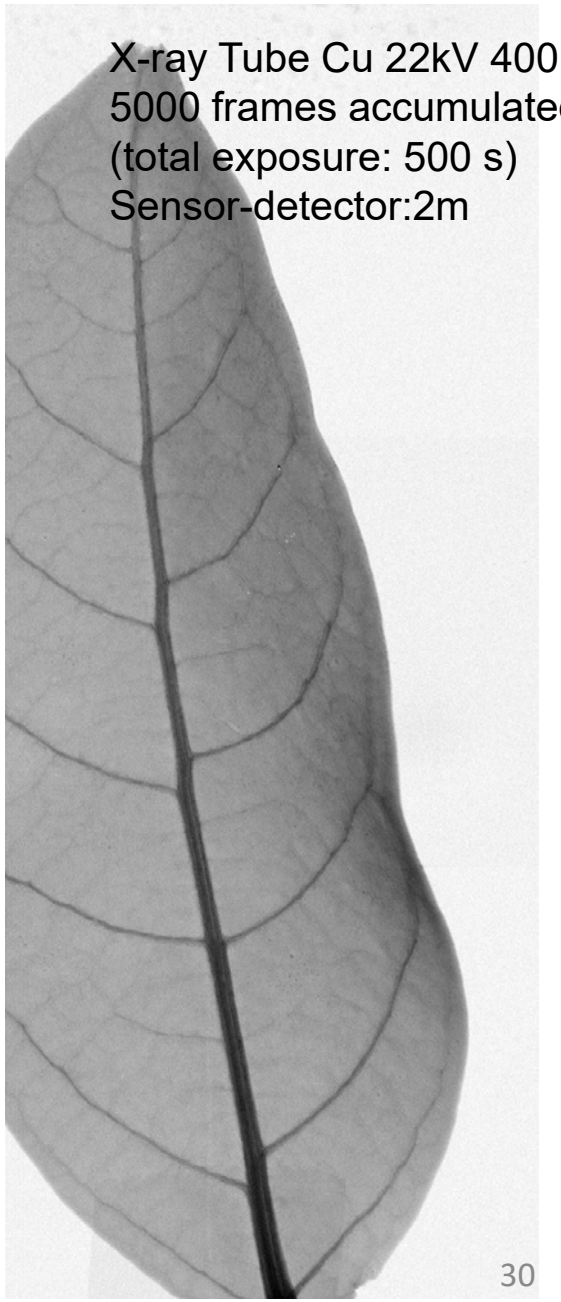
# SOI Photon-Imaging Array Sensor (*SOPHIAS*) *for* X-ray Free Electron Laser (XFEL) SACLA

Utilization of SOPHIAS has been started for various experiments in SACLA@RIKEN.

- Dynamics of Atomic Structure
- Direct Observation of Chemical Reactions
- etc.



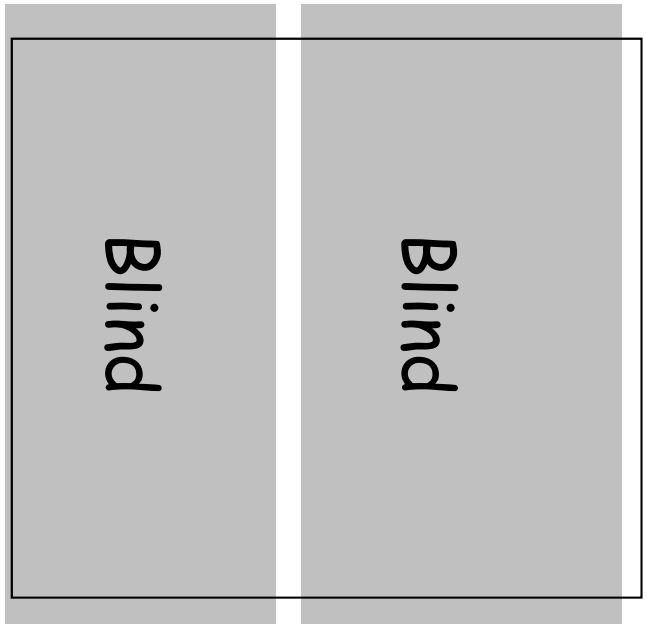

*Dual Sensor Camera*

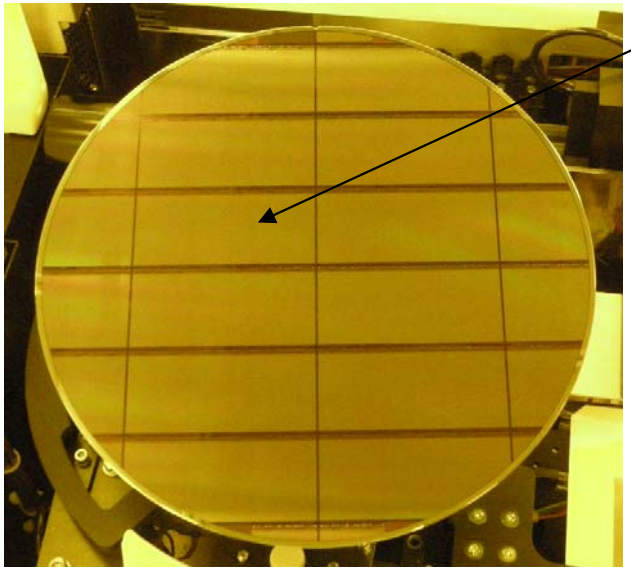


X-ray Tube Cu 22kV 400uA
5000 frames accumulated
(total exposure: 500 s)
Sensor-detector:2m

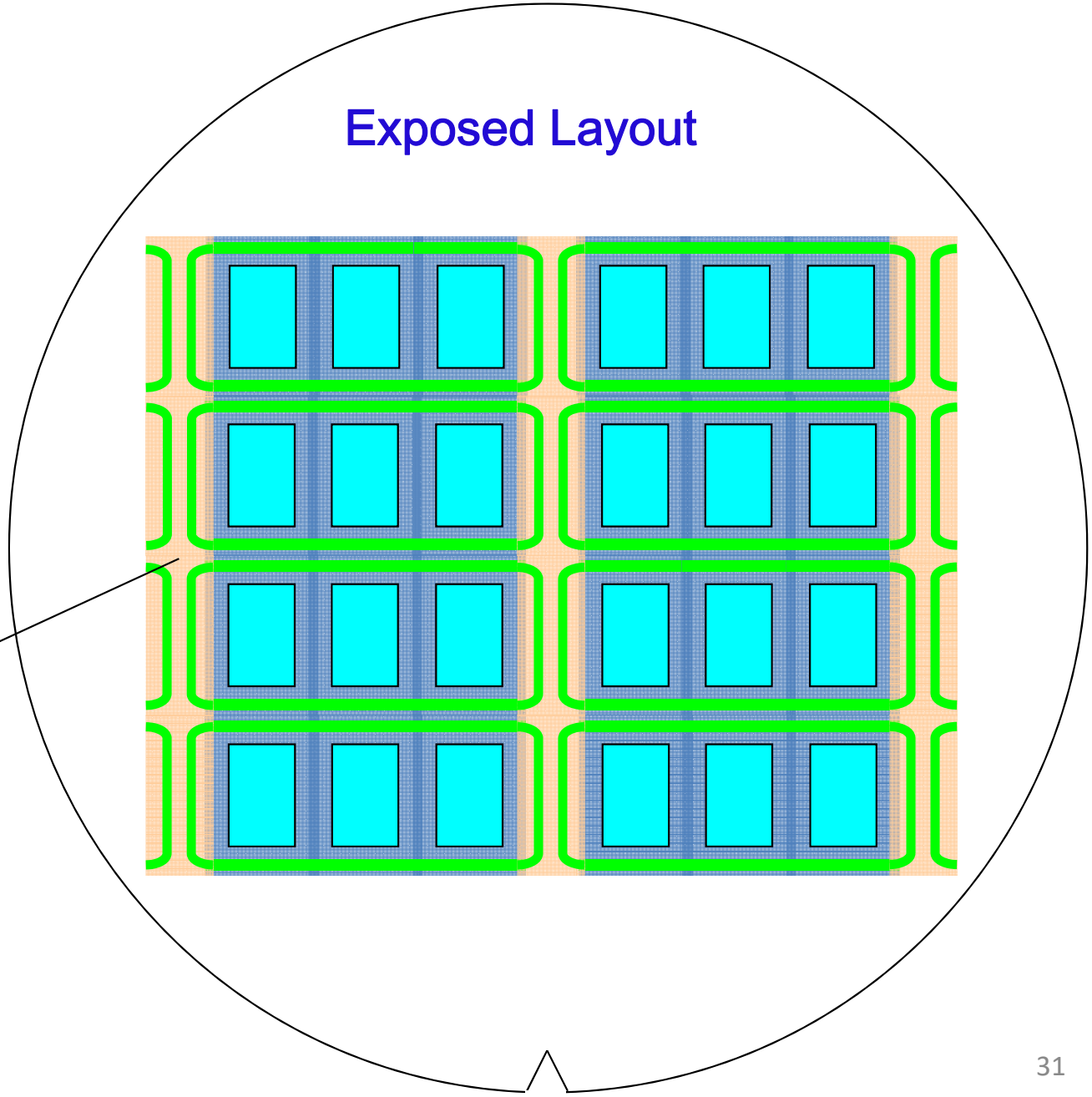
# Stitching Exposure for Large Sensor

## Mask Layout



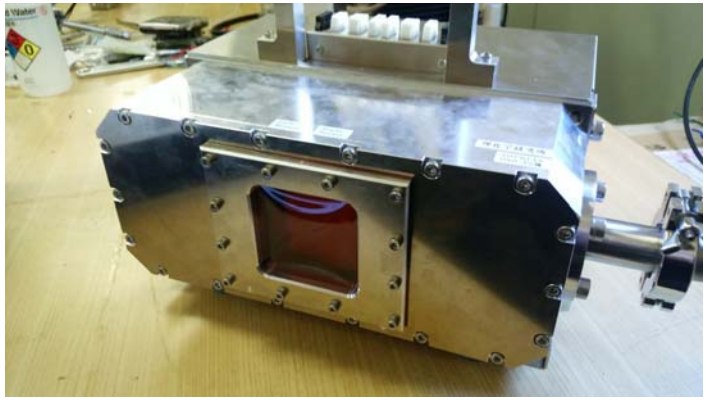



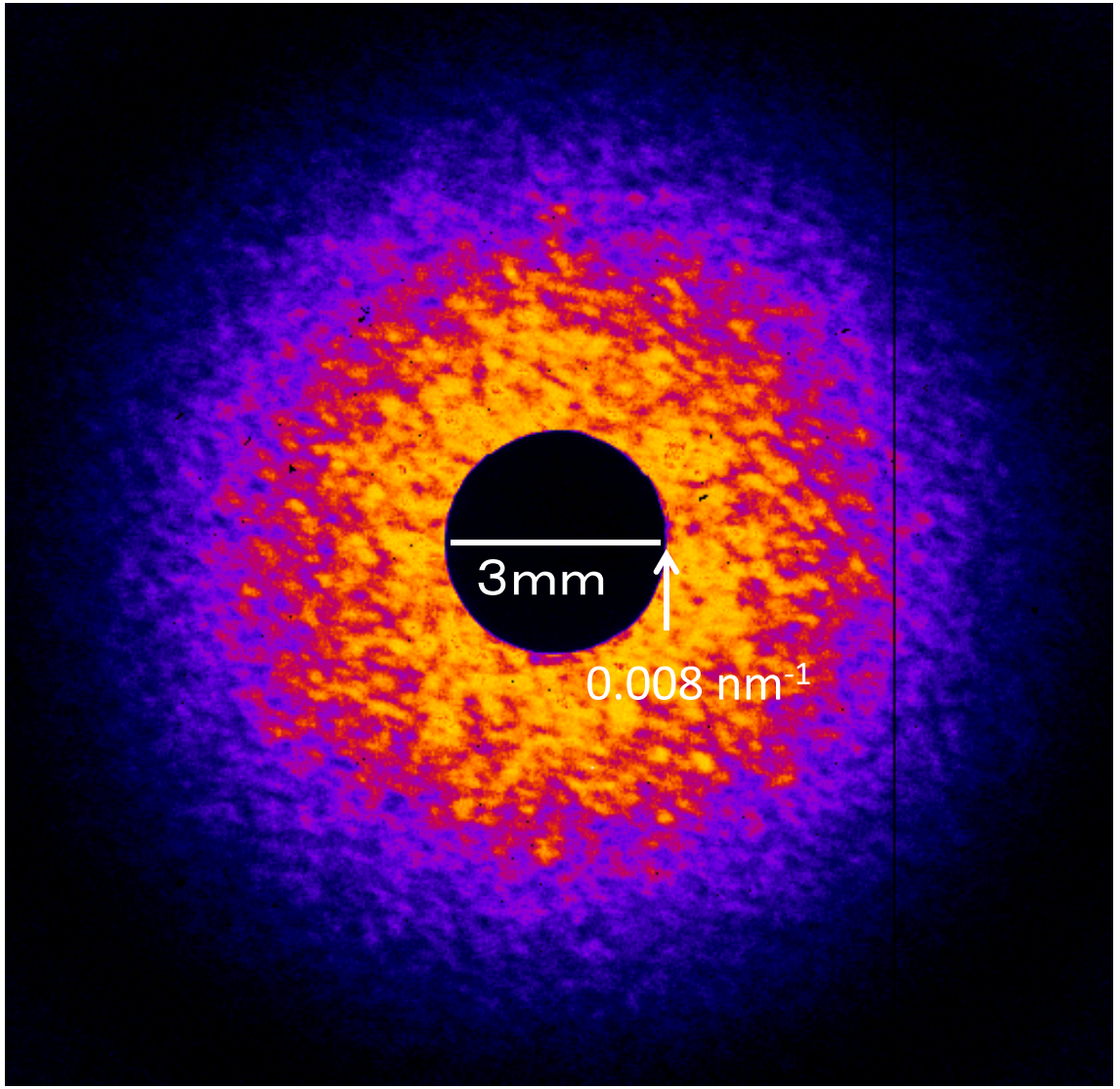
## Exposed Layout



# SOPHIAS detector: Fluctuation of speckle pattern

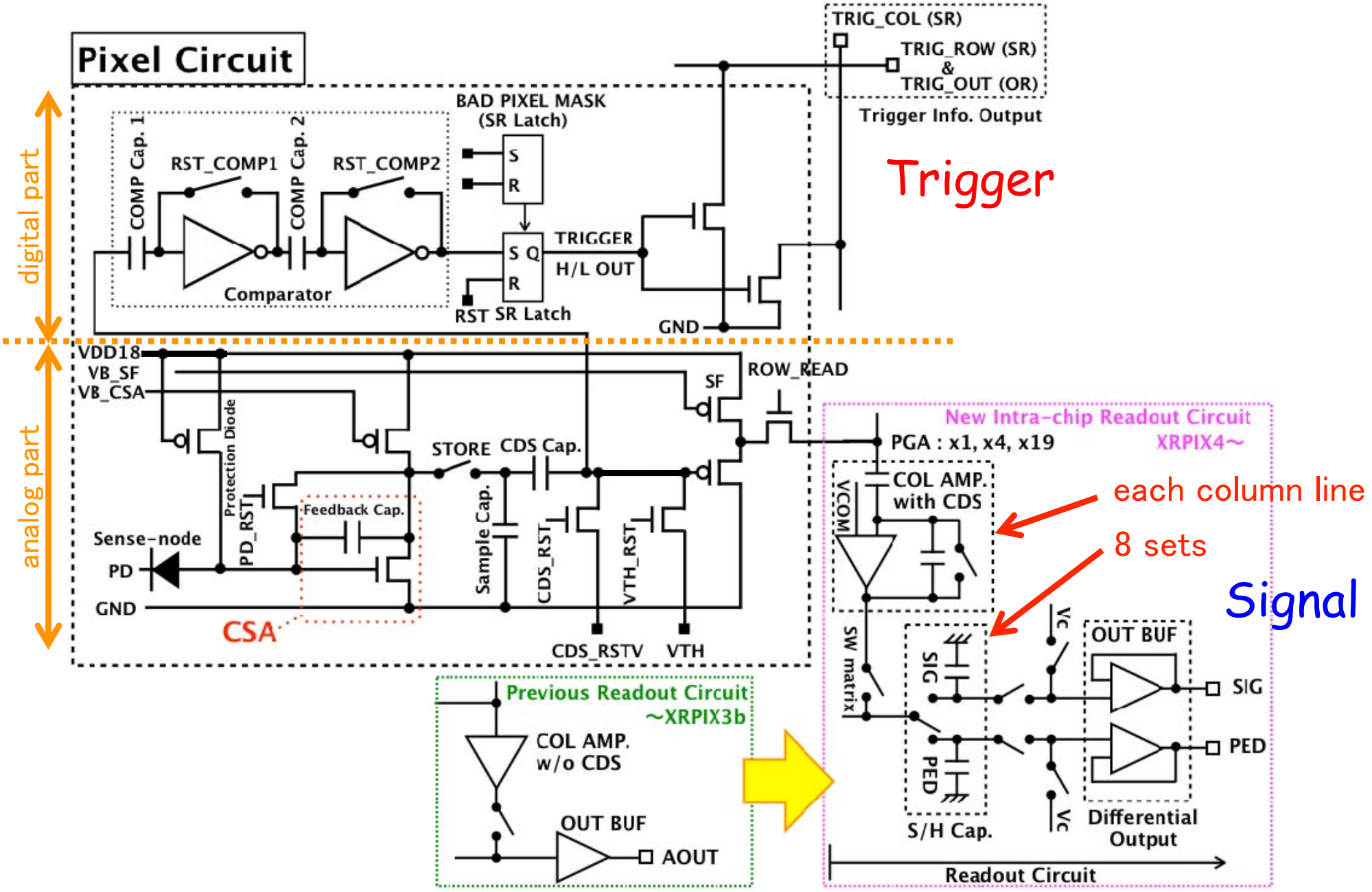
**Wave length: 0.155 nm**
**Camera length: 7.7 m**
**Beam E=8keV ϕ 30um**
**Detector:**
**SOPHIAS (30μm² / pixel)**
**Frame rate:**
**30 Hz (readout 8ms)**
**Sample:**
**200 nm Si particle in PPG**



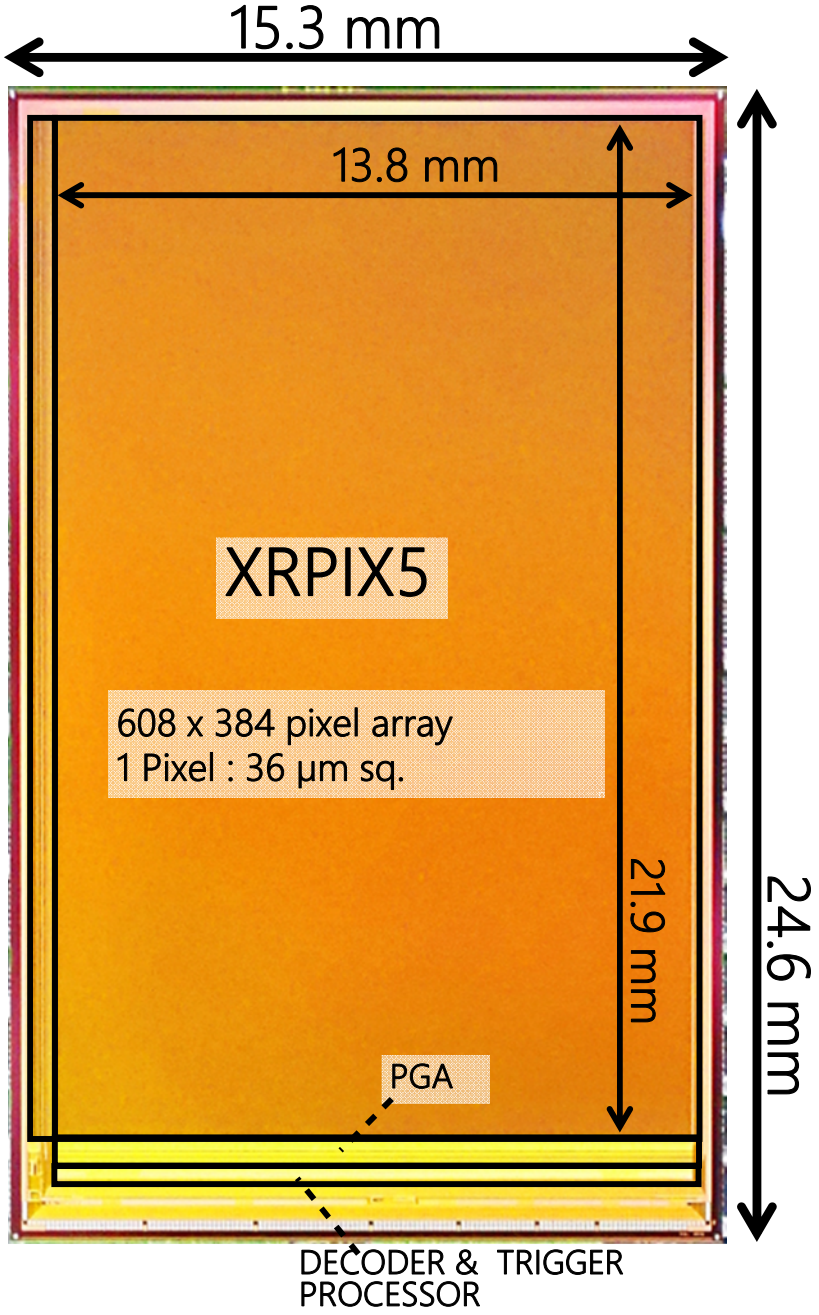



Courtesy of Prof. Masunaga and Dr. Kudo.

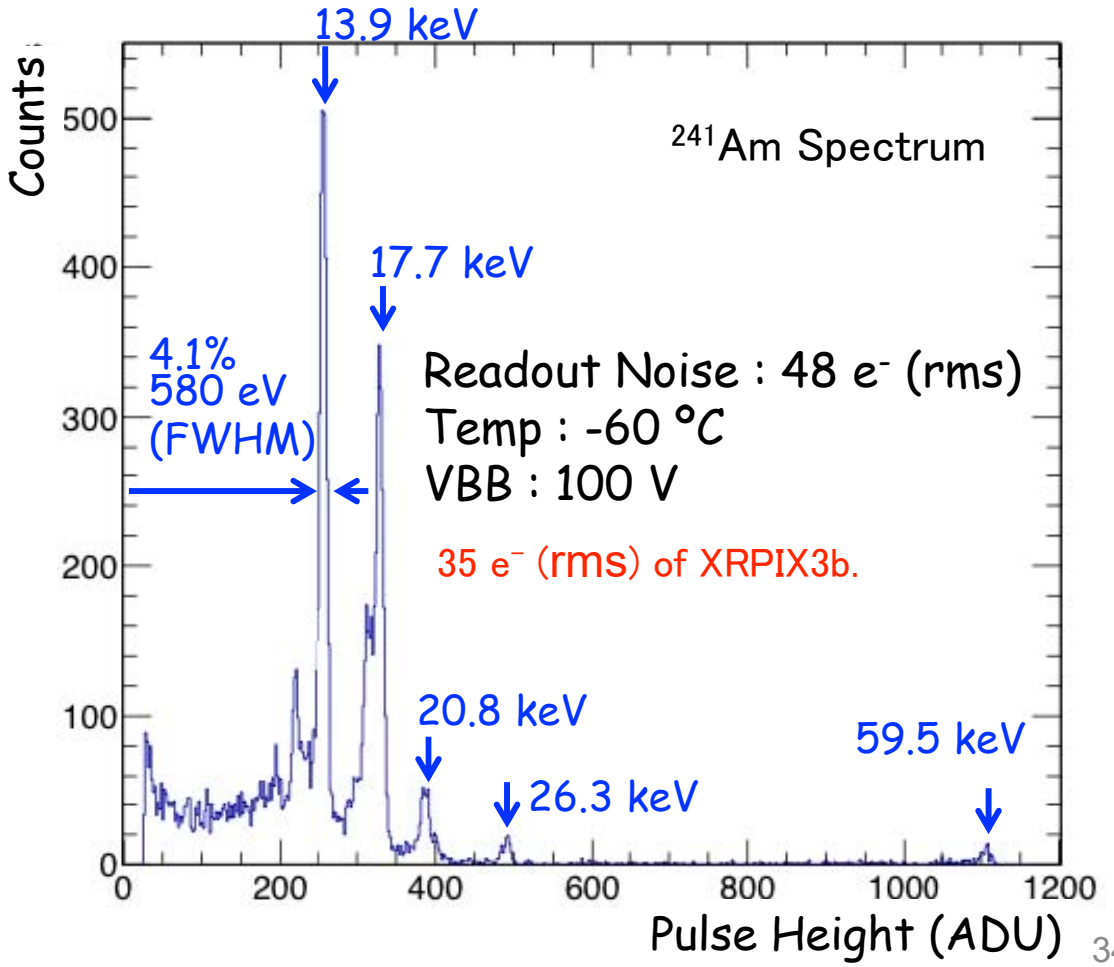
# XRPIX5: Event Driven X-ray Astronomy Detector



# XRPIX5: Event Driven X-ray Astronomy Detector




- Chip size : 24.6 mm x 15.3 mm
- Pixel size : 36 μm sq.
- # of pixel : 608 x 384 (= ~233k)
- Thickness of sensor layer : 310 μm (CZ wafer)
  500 μm (FZ wafer)

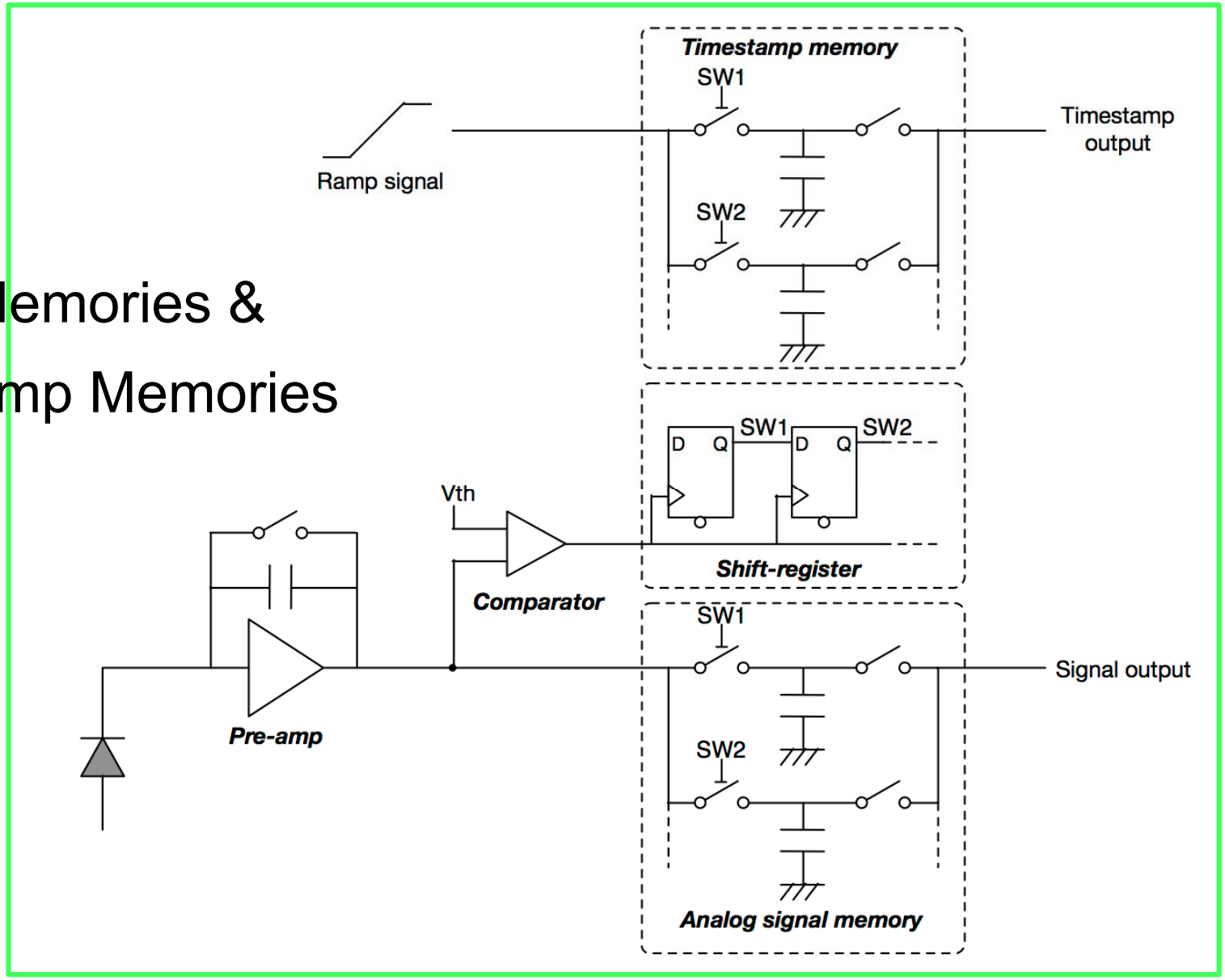


# R&D for ILC Vertex Detector

## SOFIST: SOI sensor for Fine measurement of Space and Time

Analog Memories &

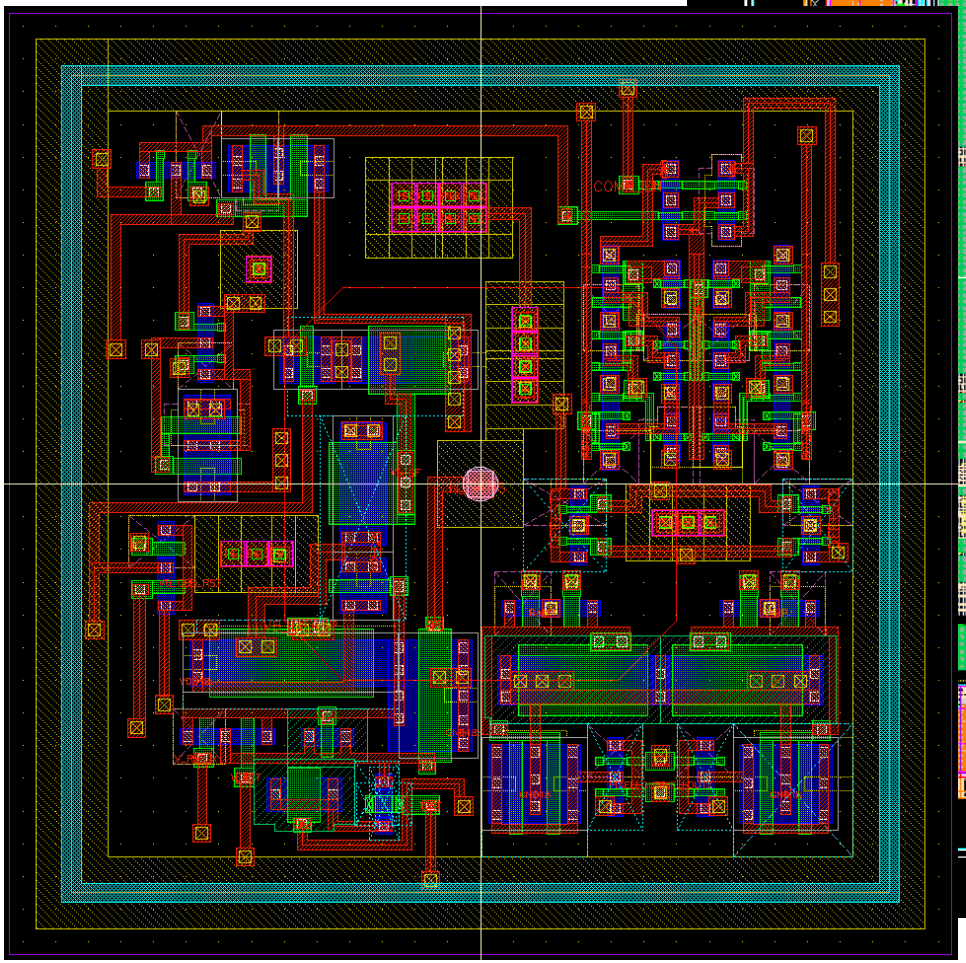
Time Stamp Memories

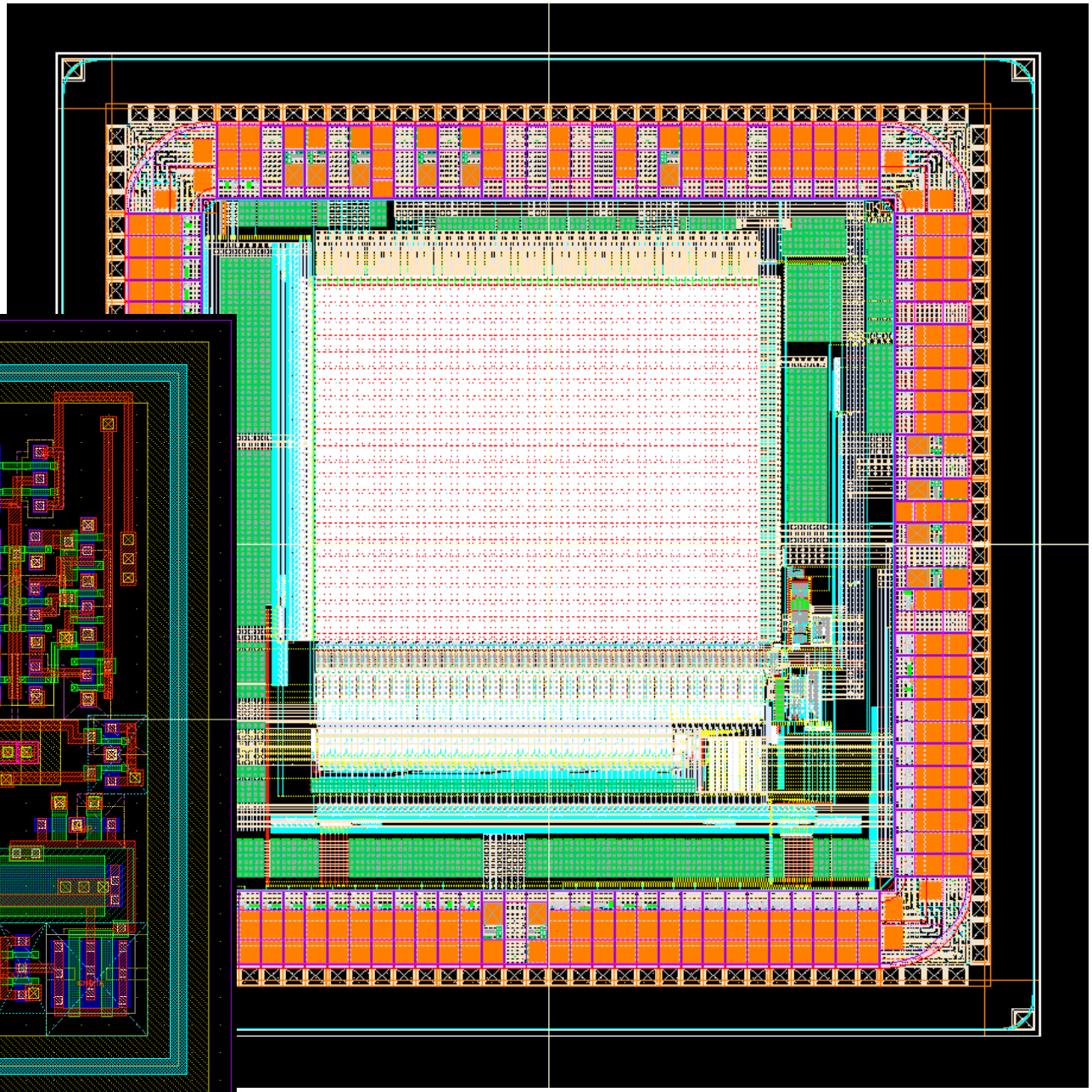


# SOFIST Test Chip (Ver.2)

Submitted last June

25um x 25um





# IV. Summary

- SOI pixel technology becomes mature. Back-gate and sensor-circuit coupling issues are solved by introducing double SOI wafer.
- Radiation tolerance is improved to more than 10 Mrad by biasing middle Si of the DSOI and increasing the dose of LDD region.
- NMOS-PMOS active merge reduces layout size very much. This is almost equivalent to go to finer process while keeping analog voltage of 0.2um process (1.8V/3.3V).
- Many kinds of SOI X-ray detectors are developed (or under development) so far.
- New R&D for ILC pixel detector (SOFIST) is started from last year.