SOI Monolithic Pixel Technology for Radiation Image Sensor

Dec. 5, 2017, IEDM@San Francisco

Yasuo Arai, T. Miyoshi and I. Kurachi
on behalf of SOIPIX Collaboration

High Energy Accelerator Research Organization (KEK)
yasuo.arai@kek.jp, http://rd.kek.jp/project/soi/
Outline of Presentation

• Introduction
• SOI Pixel Process
  3 process refinements
  - Buried Well
  - Double SOI
  - Pinned Depleted Diode
• Performance Examples of the Detector
• Summary
Introduction

Compton Electrons Tracks observed in the SOIPIX.
High Energy Accelerator Research Organization (KEK)

Research on Fundamental Science by using Particle Accelerator

Belle Detector
KEK Facilities. (www.kek.jp)

KEK Tokai, J-PARC (30 GeV Proton)

KEK Tsukuba
Super KEKB (4 GeV e⁺ - 7 GeV e⁻)
Photon Factory (2.5 & 6.5 Gev Sync. Rad.)

International Linear Collider Project (~1TeV e⁺ - e⁻, planned at Iwate)
Semiconductor Radiation Detectors are one of main R&D item in our research field.

The Detector must be
• High Resolution (Position, Energy, Time)
• High Detection Efficiency
• Radiation Tolerance
• Power consumption
• ....
Interaction between Silicon and Radiation

Visible Light (~2 eV)

- ~ 1 e-h / 1 Photon

X-ray (1-30 keV)

- ~ 300 e-h / 10 keV
- Need thick depletion region to get high efficiency for X-ray
- Collect all e-h to obtain good energy resolution.

High Energy Charged Particle (> 1Gev)

- ~ 80 e-h / 1 μm
- Small material not to deflect the particle direction.
- Measure charge distribution to get better position resolution.
Present Silicon Pixel Detector (Hybrid Pixel)

- Sensor and Readout LSI are bump bonded.
- Pixel size is limited by the bump size
- High Cost, Low Productivity in bonding
- Dead materials ...

Monolithic Radiation Detector
SOI technology looks ideal to realize the monolithic pixel detector. To use SOI technology for pixel detector is already discussed in 1990(*).

Main issues in SOI Pixel

- Transistors does not work when high-voltage is applied to handle wafer.  
  (Back-Gate Effect)
- Circuit signal and sense node couples.  
  (Signal Cross Talk)
- Oxide trapped hole induced by radiation will shift transistor threshold voltage.  
  (Radiation Tolerance)

Unfortunately, in 1990s, due to immature process technology, no good high-resistivity SOI wafer etc., many SOI sensor R&D projects were abandoned.
SOI Pixel Process

(from SOITEC Web)
Our challenge for SOIPIX have started in 2005. Monolithic Detector having fine resolution of silicon process and high functionality of CMOS LSI by using a SOI Pixel Technology.
Features of SOI Pixel Detector

• Monolithic device. No mechanical bonding. Small pixel size.

• Fabricated with semiconductor process only.
  ⇒ High reliability and Low Cost.

• High Resistive fully depleted sensor (50um~700um thick) with Low sense node capacitance. ⇒ Large S/N.

• On Pixel processing with CMOS circuits.

• No Latch up and very low Single Event cross section.

• Can be operated in wide temperature (1K-570K) range.

• Based on Industry Standard Technology.
### Lapis Semiconductor 0.2 μm FD-SOI Pixel Process

| Process | 0.2 μm Low-Leakage Fully-Depleted SOI CMOS  
1 Poly, 5 Metal layers.  
MIM Capacitor (1.5 fF/um²), DMOS  
Core (I/O) Voltage = 1.8 (3.3) V |
| SOI wafer (single) | Diameter: 200 mmφ, 720 μm thick  
Top Si : Cz, ~10 Ω-cm, p-type, ~40 nm thick  
Buried Oxide: 200 nm thick  
Handle wafer: Cz (n) ~700 Ω-cm,  
FZ(n) > 2k Ω-cm, FZ(p) ~25 k Ω-cm etc. |
| Backside process | Mechanical Grind, Chemical Etching, Back side Implant, Laser Annealing and Al plating |
SOIPIX MPW (Multi-Project Wafer) run

We are operating 1-2 times/year for academic users.

Mask Size 24.6 x 30.8 mm
• Make P-N junction by cutting top SOI Si and BOX.
• Then implant impurity with high density.

With biasing high-voltage to the backside of substrate, Leakage current will increases.
**1st refinement: Buried p-Well (BPW)**

- Suppress the **Back Gate Effect**.
- Shrink pixel size without loosing sensitive area.
- Increase break down voltage with low dose region.
- With biasing middle Si layer, radiation hardness is improved.

---

**BPW Implantation**

- Keep Top Si not affected
- Low Dose

---

**NMOS Ids – Vgs with BPW=0V**

- Low Dose BPW Implantation
- Pixel
- Peripheral
- BPW

---

**Graph**

- NMOS Ids vs. Vgs with BPW=0V
- Vback= 0V, 5V, 10V, 50V, 100V
- Log-log scale
Main Issues in SOI detector (cont.)

The BPW layer solved the back gate issue, but other issues are not yet solved.

Then we introduced additional conductive layer under the transistors (→ Double SOI).
• Middle Si layer shields coupling between sensor and circuit.
• It also compensate E-field generated by radiation trapped hole by applying negative voltage to the middle layer.
• Possible to shrink buried well size to reduce sensor capacitance.
Specifications of the Double SOI wafers

<table>
<thead>
<tr>
<th></th>
<th>1st (SOITEC)</th>
<th>2nd (Shinetsu)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SOI1</td>
<td>p-type 88 nm, &lt; 10 Ω • cm</td>
<td>p-type 88 nm, &lt; 10 Ω • cm</td>
</tr>
<tr>
<td>BOX1</td>
<td>145 nm</td>
<td>145 nm</td>
</tr>
<tr>
<td>SOI2</td>
<td>p-type 88 nm, &lt; 10 Ω • cm</td>
<td>n-type 150 nm, 3-5 Ω • cm</td>
</tr>
<tr>
<td>BOX2</td>
<td>145 nm</td>
<td>145 nm</td>
</tr>
<tr>
<td>Substrate</td>
<td>n-type Cz, 725um, ~700 Ω • cm</td>
<td>p-type FZ, 725um, &gt; 5.0 k Ω • cm</td>
</tr>
</tbody>
</table>

N-type middle Si layer has lower sheet resistance with negative SOI2 layer voltage, since P-type layer become depleted.
TEM image of the DSOI.

Cross section of the Double SOI Pixel

- Transistor
- Middle Si
- Metal 1
- Sensor Contact
- Middle Si Contact
- Metal 5
Cross Talk Reduction in Double SOI

Cross Talk from Clock line

Cross Talk between Circuit and Sensor is reduced to 1/20.

(Lu Yunpeng (IHEP))
Radiation Hardness Improvement in DSOI
(Id-Vg Characteristics v.s. SOI2 Potential)

By setting Middle Si potential (Vsoi2) to -5V, Id-Vg curve returned nearly to pre-irradiation value at 100 kGy(Si) (10 Mrad).

(U. of Tsukuba)
Radiation Hardness Improvement in DSOI
(Ids-Vgs Characteristics v.s. SOI2 Potential)

I/O Normal Vt
Source-Tie
L/W = 0.35um/5um

Threshold voltage shift is not so sensitive to radiation dose and the middle Si potential. However, Drain Current decreases by 80% at 100 kGy(Si).

(U. of Tsukuba)
Dose Increase in Lightly Doped Drain (LDD) Region

- Major cause of the drain current degradation in PMOS with radiation is $V_{th}$ increase at gate edge due to positive charge generation in spacer.
- Charge in spacer control the $V_{th}$ of the parasitic transistor.
- To reduce this effect, lightly doped drain (LDD) dose should be increased.
- Present process has rather low dose in LDD region to aiming lower power.

![Diagram of Parasitic Transistor and LDD Region](image-url)
Recovery of the drain current reduction

By increasing Implantation dose of PLDD region 6 times higher than present value, the degradation is reduced from 80% to 20% at 112 kGy(Si).

3\textsuperscript{rd} refinement: Pinned Depleted Diode (SOIPIX-PDD)

There are relatively large surface leakage current.

Leakage current between BOX and Substrate is pinned with BPW while avoiding punch throw with deep BNW layer.

(H. Kamehama et al., ‘A Low-Noise X-ray Astronomical SOI Pixel Detector Using a Pinned Depleted Diode Structure, to be published in Sensors.)
Performance Examples of the SOIPIX Detector

3D Computed Tomography with Syncrotron X-ray measured with SOIPIX
Energy Resolution:
X-ray Spectrum of $^{55}$Fe using the SOIPIX-PDD

Gain = 70 $\mu$V/e-
Noise = 11.0 e-
Dark Current = 56 pA/cm² @-35°C

Very good Resolution (low noise) and no tail in the peak (showing perfect charge collection efficiency).
Tracking Resolution: High-Energy Beam test @Fermi National Accelerator Lab.

Two kinds of SOIPIX-DSOI detectors are used:
- FPIX2 x 4: 8 μm square pixel detector
- SOFIST1 x 2: 20 μm square pixel detector
Less than 1 μm Position Resolution for high-energy charged particle is achieved first in the world.

(K. Hara et al., Development of Silicon-on-Insulator Pixel Detectors, Proceedings of Science, to be published)
Summary

• Process for SOI radiation pixel detector is developed. Three new refine techniques are developed to achieve high performance.
• Buried Well is very effective to shield high-voltage for sensor region.
• Double SOI technology is excellent in shielding the high-voltage and cross talk between sensor and circuit. Furthermore, with biasing negative voltage to the middle SOI layer, radiation hardness is improved more than 100 kGy(Si).
• With Pinned Depleted Diode (PDD) structure, Leakage current is reduced to less than 60 pA/cm², and very good charge collection efficiency and low noise is obtained.
• Many kinds of SOI radiation detectors are being developed for various scientific applications.